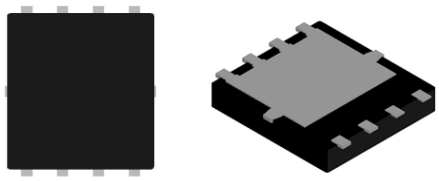
SPM0614DNAQ

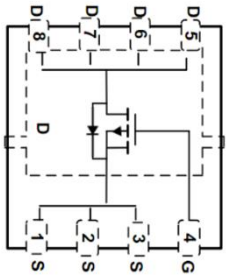
Single P-Channel, -60V, -64A, Power MOSFET

http://www.sitcores.com/

V_{DS} (V)	Max. $R_{DS(on)}$ (mΩ)
-60	14 @ V_{GS}=-10V
	22 @ V_{GS}=-4.5V



PDFN5X6-8L



Pin Configuration (Top view)

Description

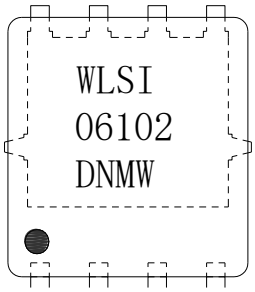
The SPM0614DNAQ is P-Channel enhancement MOS Field Effect Transistor. Uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. This device is suitable for use in high performance automotive DC-DC conversion, power switch and charging circuit. Standard Product SPM0614DNAQ is in compliance with RoHS.

Features

- Automotive applications
- AEC-Q101 Qualified
- Excellent ON resistance
- General footprint package PDFN5X6-8L
- 100% Rg and Avalanche tested
- MSL1

Applications

- Automotive systems
- DC/DC converters
- Power supply converters circuit
- Load/Power Switching for portable device



WLSI = Company (Group) Code
06102 = Device Code
DN = Special Code
M = Month
W = Week

Marking

Order information

Device	Package	Shipping
SPM0614DNAQ-8/TR	PDFN5*6-8L	5000/Tape& Reel

Absolute Maximum ratings (T_J=25℃, unless otherwise noted)

Parameter		Symbol	Maximum	Unit
Drain-Source Voltage		V_{DS}	-60	V
Gate-Source Voltage		V_{GS}	-20V/+12V	
Continuous Drain Current	T_C=25°C	I_D	-64	A
	T_C=100°C		-45	A
Pulsed Drain Current [c]		I_{DM}	-163	A
Continuous Drain Current	T_A=25°C	I_D	-11.2	A
	T_A=100°C		-7.9	
Avalanche Energy L=0.1mH		E_{AS}	304	mJ
Power Dissipation [b]	T_C=25°C	P_D	109	W
	T_C=100°C		55	
Power Dissipation [a]	T_A=25°C	P_D	3.4	W
	T_A=100°C		1.7	
Operating Junction Temperature		T_J	-55 to 175	°C
Storage Temperature Range		T_{STG}	-55 to 175	°C

Thermal resistance ratings

Single Operation					
Parameter		Symbol	Typical	Maximum	Unit
Junction-to-Ambient Thermal Resistance [a]	Steady State	$R_{\theta JA}$	37	44	°C/W
Junction-to-Case Thermal Resistance [b]	Steady State	$R_{\theta JC}$	1.0	1.4	

Note:

a FR-4 board (38mm X 38mm X t1.6mm, 70um Copper) partially covered with copper (645mm^2 area). The power dissipation P_{DSM} is based on Junction-to-Ambient thermal resistance value and the $T_{J(MAX)}$=175°C. The value is only for reference, any application depends on the user's specific board design.

b The power dissipation P_D is based on $T_{J(MAX)}$=175°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heat sinking is used.

c Repetitive rating, pulsed, duty cycle ~1%, keep initial T_J =25°C, the maximum allowed junction temperature of 175°C.

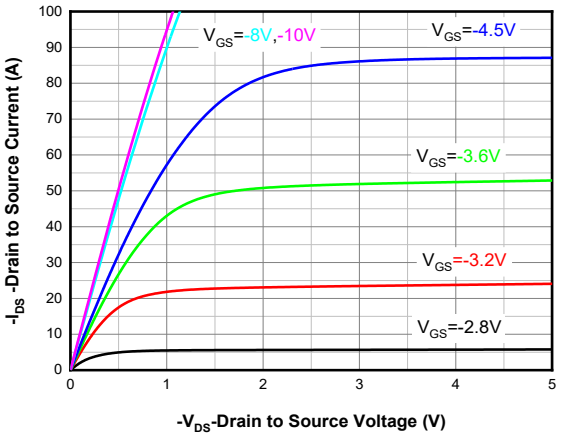
d The static characteristics are obtained using ~380us pulses, duty cycle ~1%.

e The parameter is not subject to production test – verified by design / characterization.

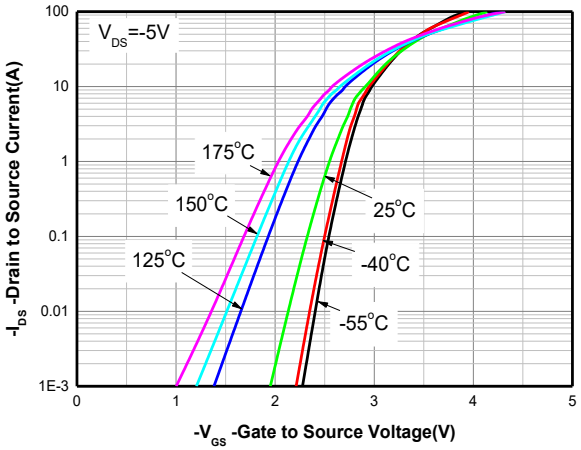
Electronics Characteristics (T_J=25°C, unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D = -250uA	-60			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	BV_{DSS}/T_J			-45		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-60V, V_{GS}= 0V, T_J=25°C			-1	uA
		V_{DS}=-60V, V_{GS}= 0V, T_J=125°C			-10	uA
Gate-to-source Leakage Current	I_{GSS}	V_{DS}=0V, V_{GS}=-20V			-100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS}=V_{DS}, I_D=-250uA	-1.5	-2	-2.5	V
Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			5		mV/°C
Drain-to-source On-resistance [d]	$R_{DS(on)}$	V_{GS} =-10V, I_D =-17A		10.5	14.0	mΩ
		V_{GS} = -4.5V,I_D =-17A		14.0	22.0	
CHARGES, CAPACITANCES AND GATE RESISTANCE						
Input Capacitance	C_{ISS}	V_{GS}=0V, f= 1.0MHz, V_{DS}=-25 V		6700		pF
Output Capacitance	C_{OSS}			500		
Reverse Transfer Capacitance	C_{RSS}			310		
Total Gate Charge [e]	$Q_{G(TOT)}$	V_{GS}=-10V V_{DS}= -48V, I_D =-17A		130		nC
Gate-to-Source Charge [e]	Q_{GS}	V_{GS}= -10V V_{DS}=-48V, I_D =-17 A		18.9		
Gate-to-Drain Charge [e]	Q_{GD}			30.5		
SWITCHING CHARACTERISTICS [e]						
Turn-On Delay Time	td(ON)	V_{GS}= -10V, V_{DS}= -48V, I_D =-17A,		9.7		ns
Rise Time	tr			36.1		
Turn-Off Delay Time	td(OFF)			230		
Fall Time	tf			81		
Body Diode Reverse Recovery Time	trr	I_F=-17A, dI/dt=-100A/μs		35		ns
Body Diode Reverse Recovery Charge	Qrr	I_F=-17A, dI/dt=-100A/μs		41		nC
BODY DIODE CHARACTERISTICS						
Forward Voltage [d]	V_{SD}	V_{GS}=0 V, I_S=-17A	-0.5	-0.8	-1.2	V

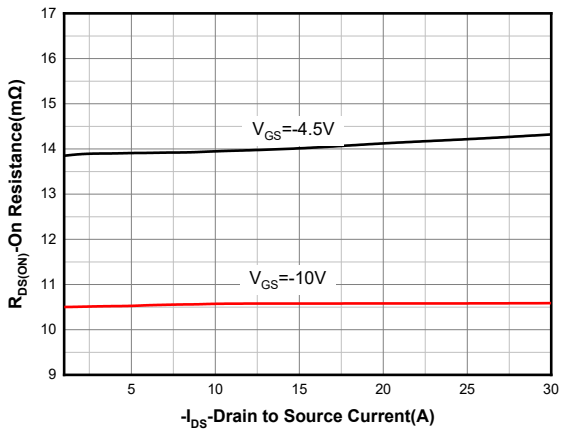
Typical Characteristics (Ta=25°C, unless otherwise noted)



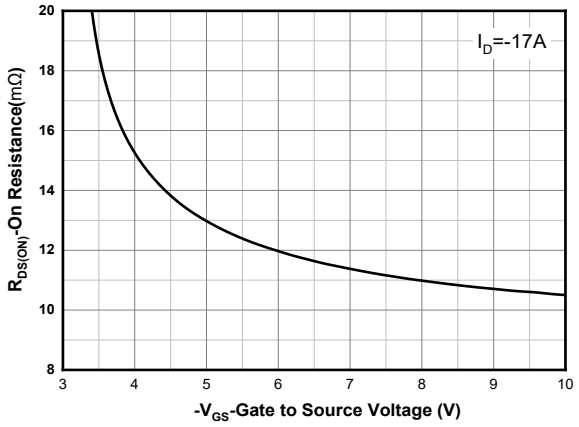
Output Characteristics [d]



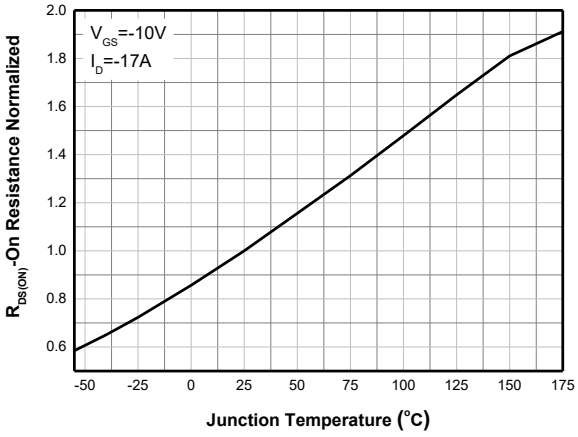
Transfer Characteristics [d]



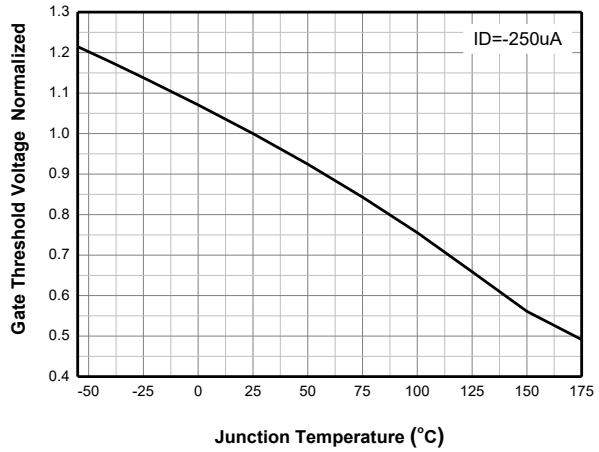
On-Resistance vs. Drain Current [d]



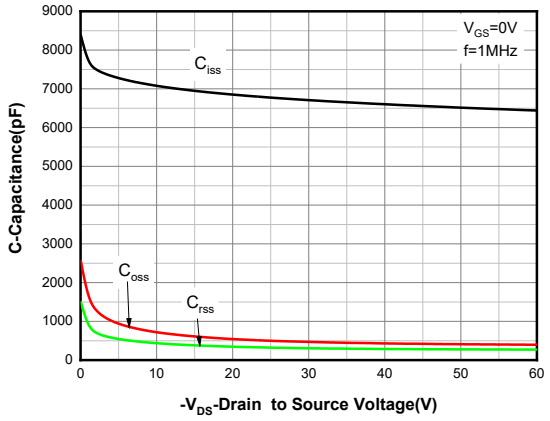
On-Resistance vs. Gate-to-Source Voltage [d]



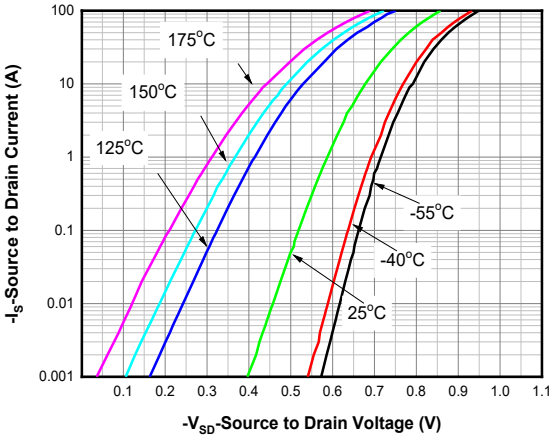
On-Resistance vs. Junction Temperature [d]



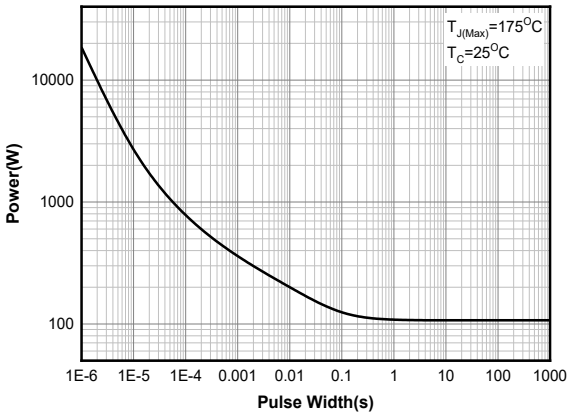
Threshold Voltage vs. Temperature



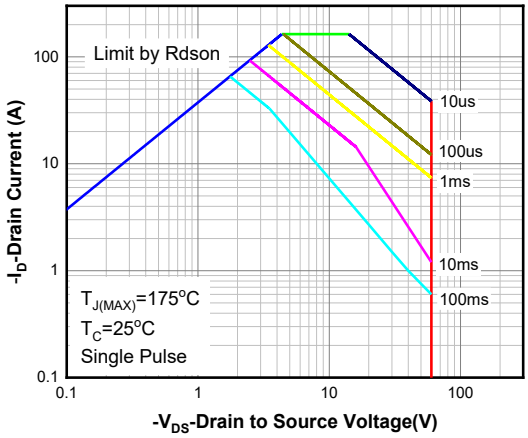
Capacitance



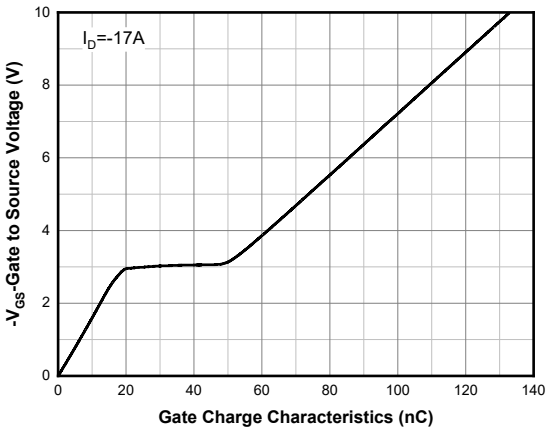
Body Diode Forward Voltage [d]



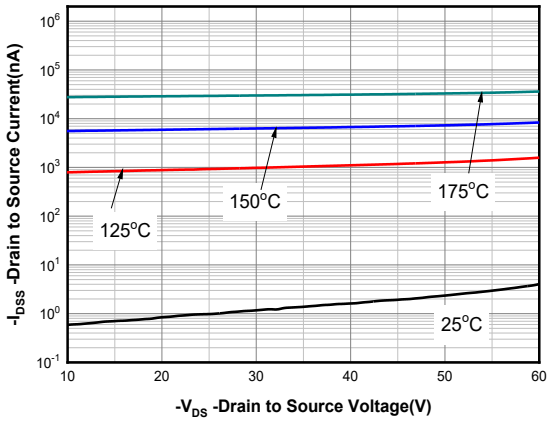
Single Pulse power



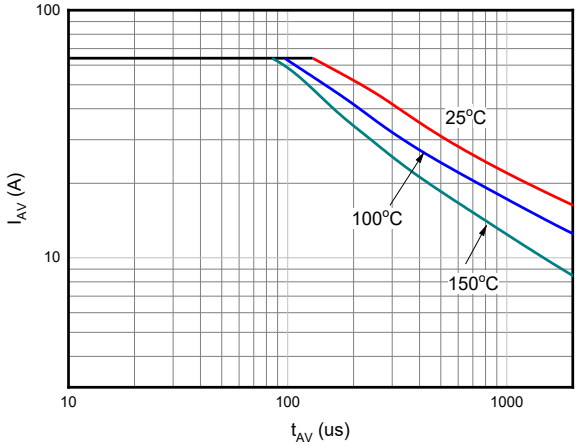
Safe Operating Area



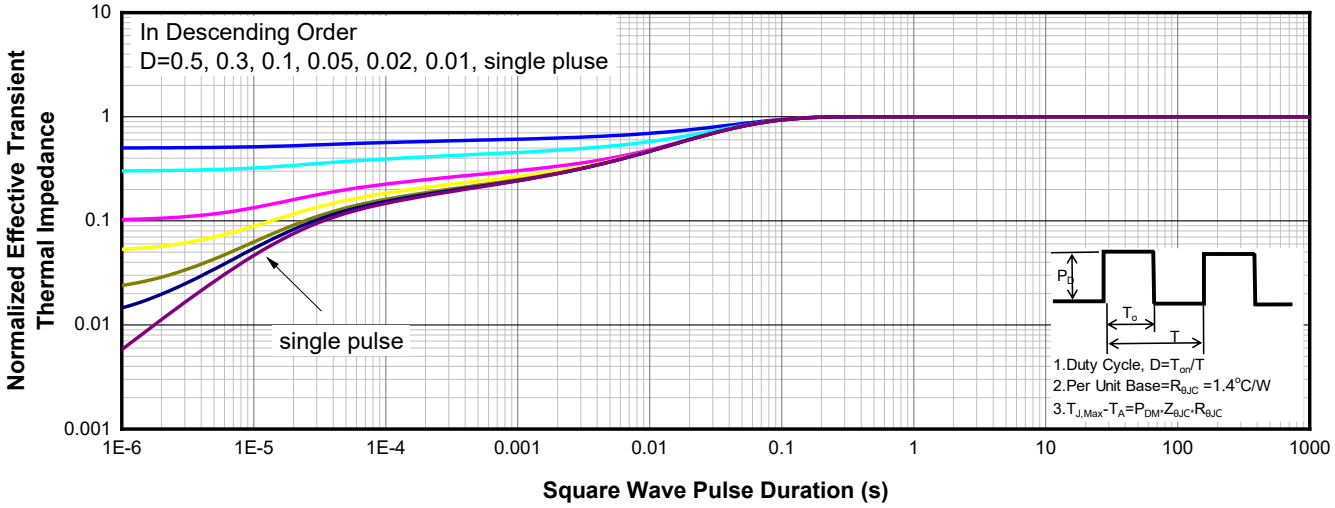
Gate Charge Characteristics



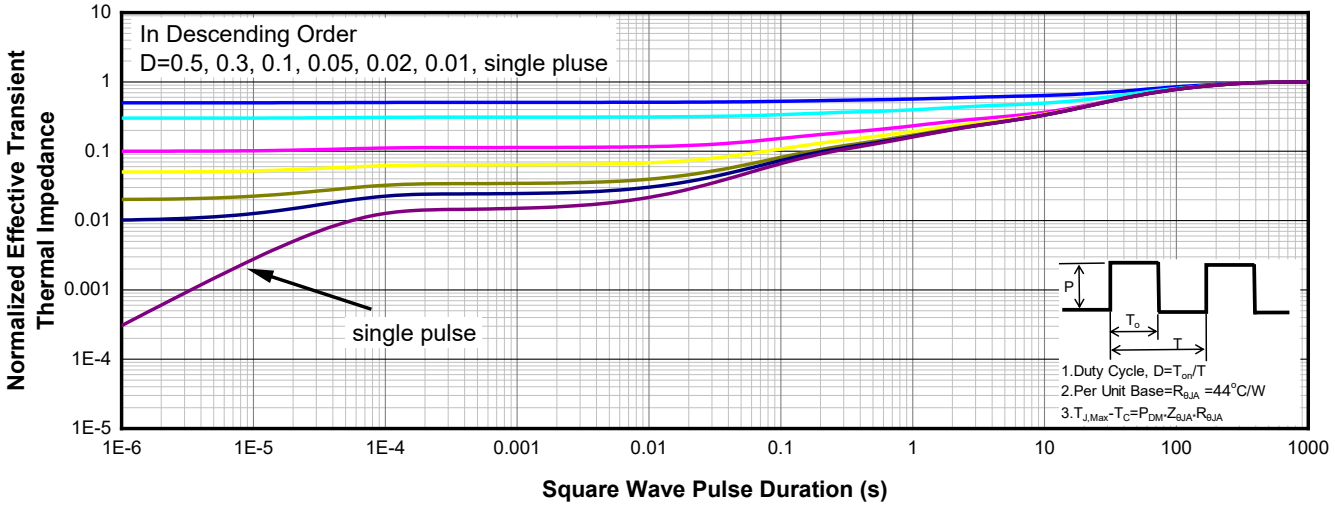
Drain Current vs. Drain Voltage



Avalanche characteristics



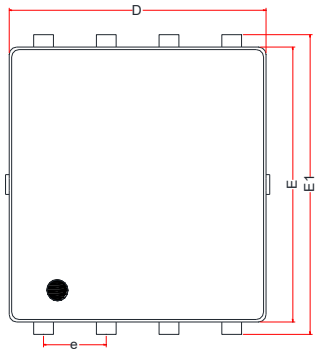
Transient Thermal Response (Junction-to-Case)



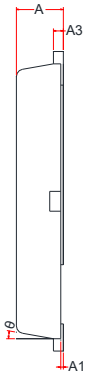
Transient Thermal Response (Junction-to-Ambient)

PACKAGE OUTLINE DIMENSIONS

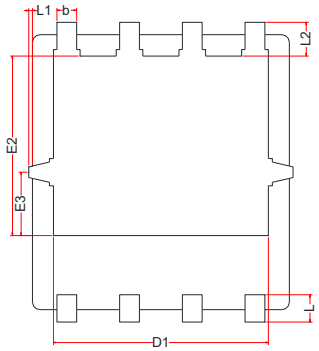
PDFN5X6-8L



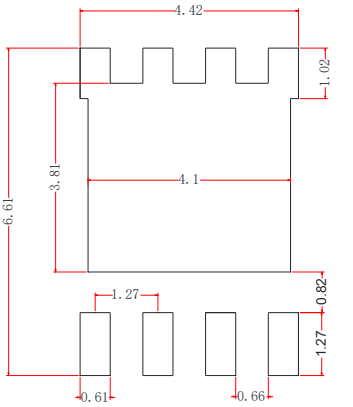
TOP VIEW



SIDE VIEW



BOTTOM VIEW

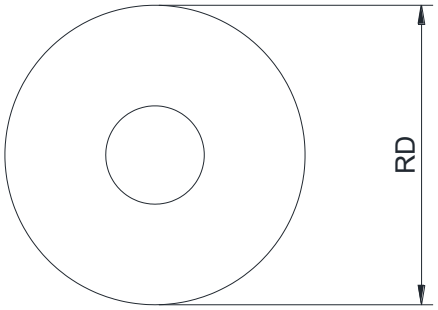


RECOMMENDED LAND PATTERN(Unit:mm)

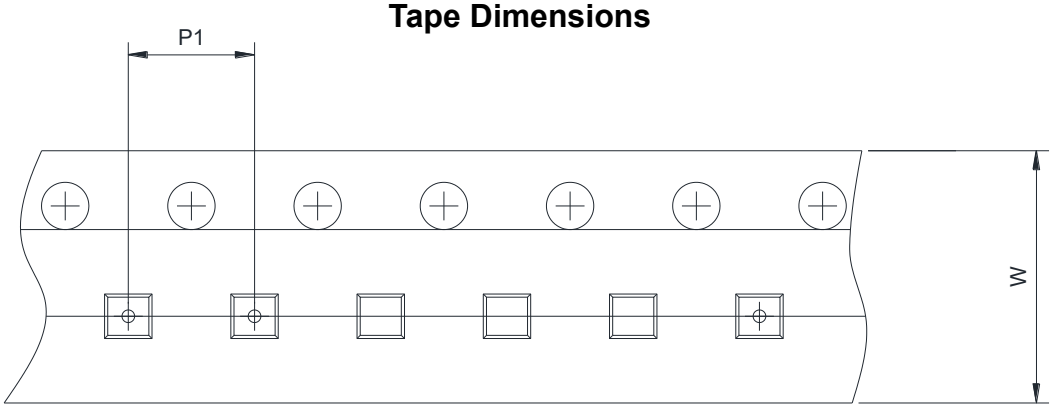
Symbol	Dimensions in Millimeters		
	Min.	Typ.	Max.
A	0.85	0.95	1.00
A1	0.00	---	0.05
A3	---	0.2 Ref	---
b	0.30	0.40	0.50
D	5.10	5.20	5.30
E	5.45	5.55	5.65
e	1.27 BSC		
D1	4.25	4.35	4.45
E1	5.95	6.05	6.15
E2	3.525	3.625	3.725
E3	1.175	1.275	1.375
L	0.45	0.55	0.65
L1	0	---	0.15
L2	0.68 Ref		
θ	0 °	---	10 °

TAPE AND REEL INFORMATION

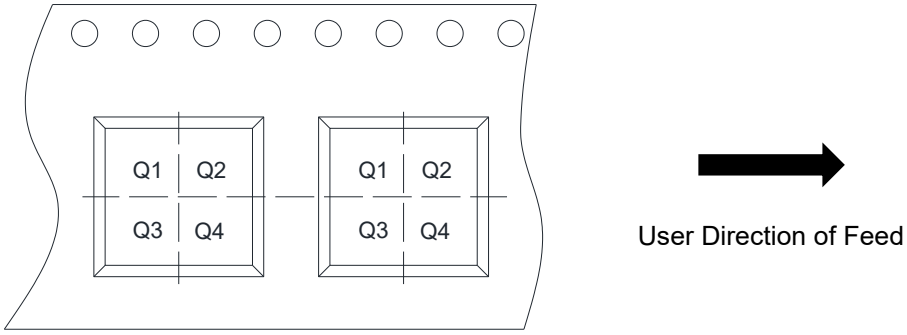
Reel Dimensions



Tape Dimensions



Quadrant Assignments For PIN1 Orientation In Tape



RD	Reel Dimension	☐ 7inch ☑ 13inch
W	Overall width of the carrier tape	☐ 8mm ☑ 12mm
P1	Pitch between successive cavity centers	☐ 2mm ☐ 4mm ☑ 8mm
Pin1	Pin1 Quadrant	☑ Q1 ☐ Q2 ☐ Q3 ☐ Q4