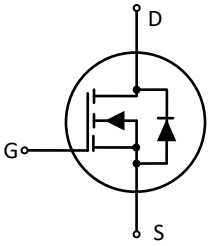
SNM104R2THA

Single N-Channel,100V,120A, Power MOSFET

http://www.sitcores.com/

V_{DS} (V)	Max. $R_{DS(on)}$ (mΩ)
100	4.2@ V_{GS}=10V

TO-263-2L



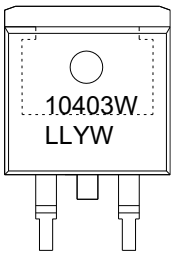
Pin configuration (Top view)

Description

The SNM104R2THA is N-Channel enhancement MOS Field Effect Transistor. Uses advanced Split Gate Trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. This device is suitable for use in DC-DC conversion, power switch and charging circuit. Standard Product SNM104R2THA is in compliance with RoHS.

Features

- Split Gate Trench Technology
- Supper high density cell design
- Excellent ON resistance
- 100% UIS and Rg Tested
- High Robustness
- MSL3



10403W = Device Code
LL = Special Code
Y = Year
W = Week (A~z)

Marking

Applications

- Hot swap
- Motor control and drive
- Battery management
- Load/Power Switching for portable device

Order information

Device	Package	Shipping
SNM104R2THA-2/TR	TO-263-2L	800/Tape&Reel

Absolute Maximum ratings

Parameter		Symbol	Maximum	Unit
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current [f]	T_C=25°C	I_D	120	A
	T_C=100°C		104	A
Pulsed Drain Current [c]		I_{DM}	267	A
Continuous Drain Current [a]	T_A=25°C	I_{DSM}	48	A
	T_A=70°C		41	
Avalanche Energy L=0.1mH		E_{AS}	320	mJ
Power Dissipation [b]	T_C=25°C	P_D	176	W
	T_C=100°C		88	
Power Dissipation [a]	T_A=25°C	P_{DSM}	19.2	W
	T_A=70°C		13.5	
Operating Junction Temperature		T_J	-55 to 175	°C
Storage Temperature Range		T_{STG}	-55 to 175	°C

Thermal resistance ratings

Single Operation					
Parameter		Symbol	Typical	Maximum	Unit
Junction-to-Ambient Thermal Resistance [a]	t ≤ 10 s	$R_{\theta JA}$	6	8	°C/W
	Steady State		32	40	
Junction-to-Case Thermal Resistance	Steady State	$R_{\theta JC}$	0.53	0.85	

Note:

a FR-4 board (38mm X 38mm X t1.6mm, 70um Copper) partially covered with copper (645mm^2 area). The power dissipation P_{DSM} is based on Junction-to-Ambient thermal resistance $R_{\theta JA}$ t≤10s value and the $T_{J(MAX)}$=175°C. The value is only for reference, any application depends on the user's specific board design.

b The power dissipation P_D is based on $T_{J(MAX)}$=175°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heat sinking is used.

c Repetitive rating, ~10us pulse width, duty cycle ~1%, keep initial T_J =25°C, the maximum allowed junction temperature of 175°C.

d The static characteristics are obtained using ~380us pulses, duty cycle ~1%.

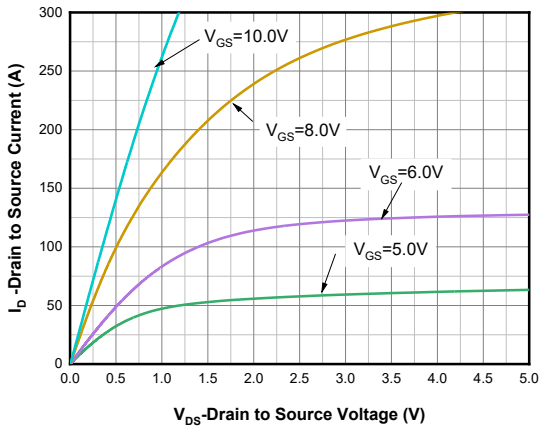
e The parameter is not subject to production test – verified by design / characterization.

f The maximum current rating by source bonding technology.

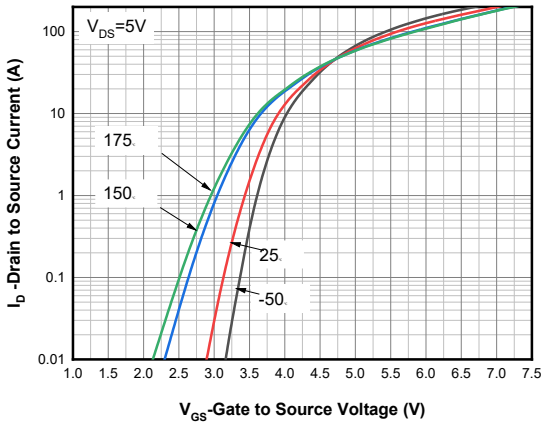
Electronics Characteristics (Ta=25°C, unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0 V, I_D= 250uA	100			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 100V, V_{GS} = 0V			1	uA
Gate-to-source Leakage Current	I_{GSS}	V_{DS}= 0V, V_{GS} = ±20V			±100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250uA	2.2	2.8	3.4	V
Drain-to-source On-resistance [d]	$R_{DS(on)}$	V_{GS} = 10V, I_D =50A		3.3	4.2	mΩ
CHARGES, CAPACITANCES AND GATE RESISTANCE [e]						
Input Capacitance	C_{ISS}	V_{GS} = 0V, f = 1.0MHz, V_{DS} = 50 V		4400		pF
Output Capacitance	C_{OSS}			1772		
Reverse Transfer Capacitance	C_{RSS}			41		
Total Gate Charge(10V)	$Q_{G(TOT)}$	V_{GS} = 10 V, V_{DD} = 50V, I_D = 50A		73.6		nC
Gate-to-Source Charge	Q_{GS}			21.2		
Gate-to-Drain Charge	Q_{GD}			18.3		
Gate Resistance	R_g	f=1MHz		1.7		Ω
SWITCHING CHARACTERISTICS [e]						
Turn-On Delay Time	td(ON)	V_{GS} = 10 V, V_{DD} = 50 V, I_D=50A, R_G = 3Ω		15.8		ns
Rise Time	tr			58		
Turn-Off Delay Time	td(OFF)			44		
Fall Time	tf			58		
BODY DIODE CHARACTERISTIC						
Forward Voltage [d]	V_{SD}	V_{GS} = 0 V, I_S = 50A		0.88	1.2	V
Body Diode Reverse Recovery Time [e]	trr	I_F=20A, dI/dt=100A/μs		87		ns
Body Diode Reverse Recovery Charge [e]	Qrr			140		nC

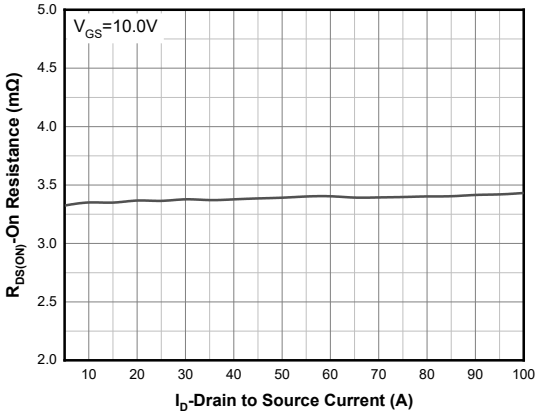
Typical Characteristics (Ta=25°C, unless otherwise noted)



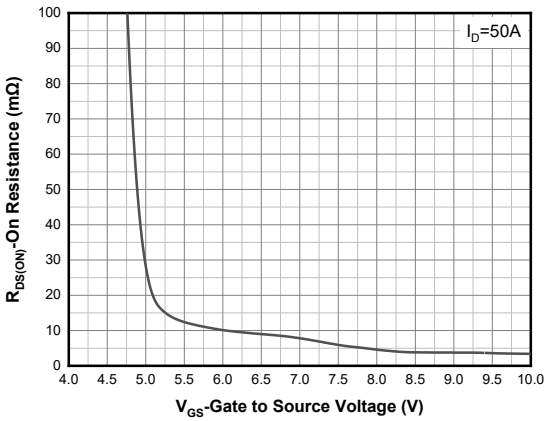
Output Characteristics [d]



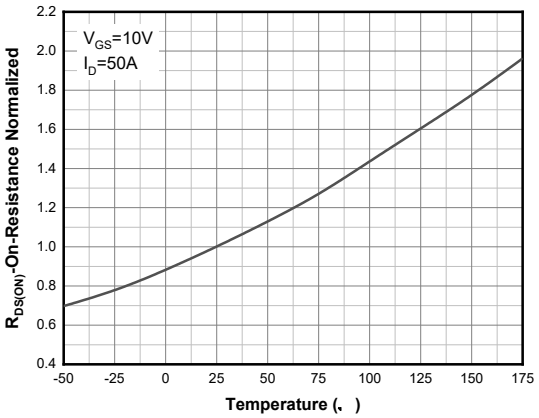
Transfer Characteristics [d]



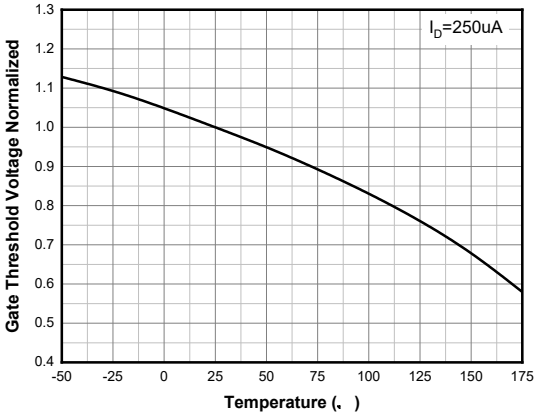
On-Resistance vs. Drain Current [d]



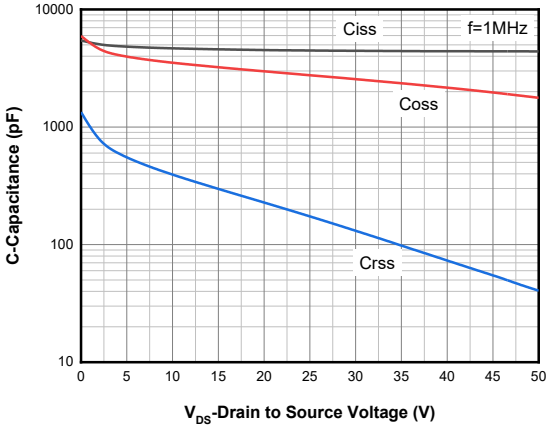
On-Resistance vs. Gate-to-Source Voltage [d]



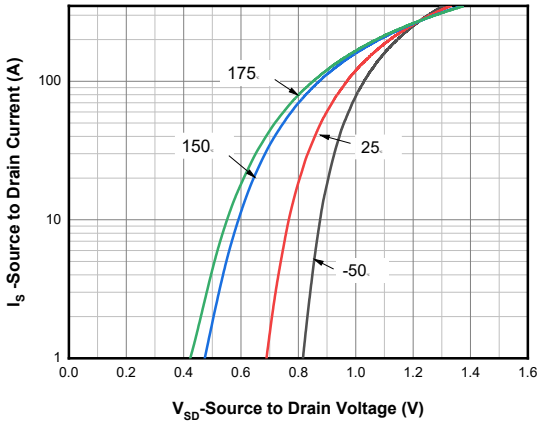
On-Resistance vs. Junction Temperature [d]



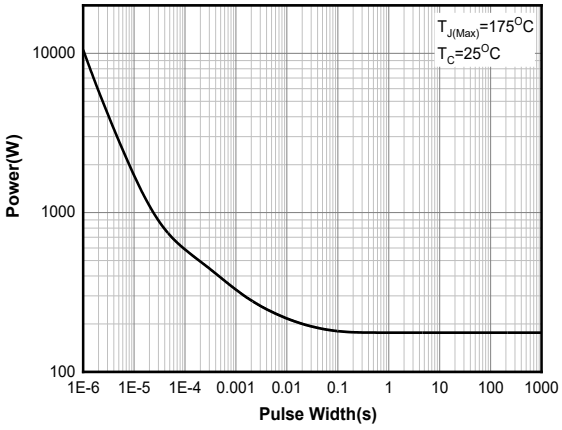
Threshold Voltage vs. Temperature



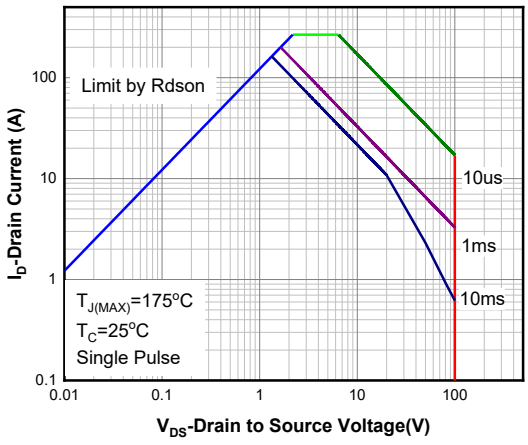
Capacitance



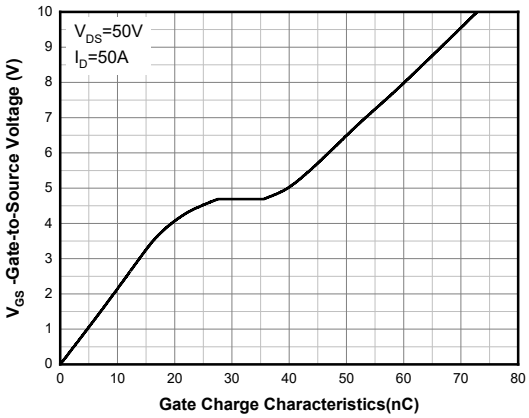
Body Diode Forward Voltage [d]



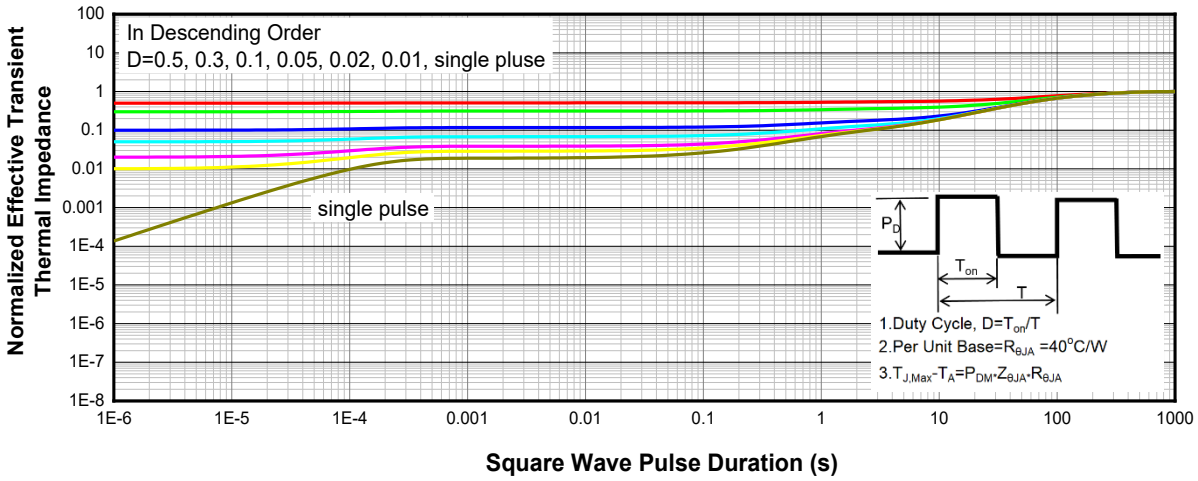
Single Pulse power



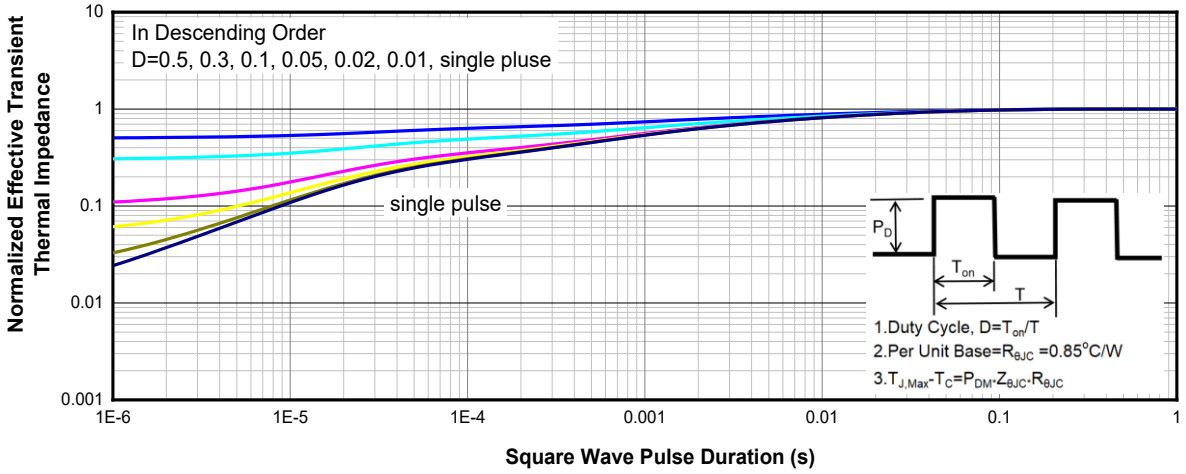
Safe Operating Area



Gate Charge Characteristics



Transient Thermal Response (Junction-to-Ambient)



Transient Thermal Response (Junction-to-Case)

PACKAGE OUTLINE DIMENSIONS

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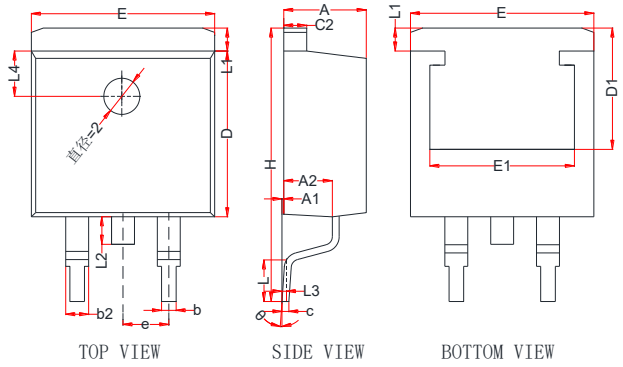
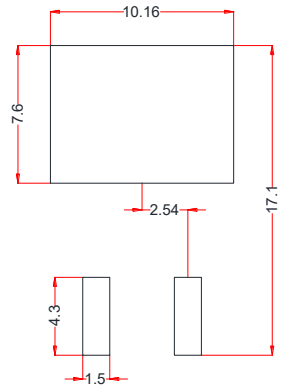


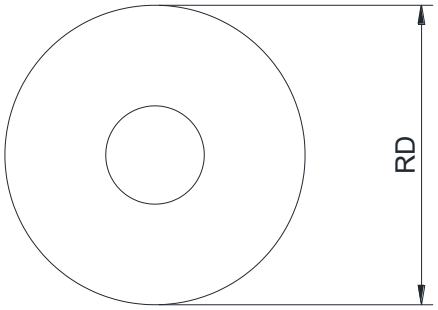


RECOMMENDED LAND PATTERN(Unit:mm)

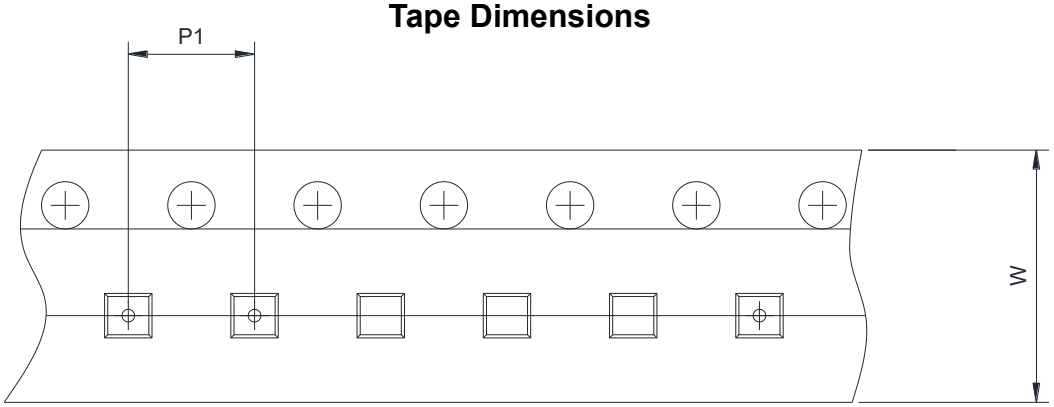
Symbol	Dimensions in Millimeters		
	Min.	Typ.	Max.
A	4.40	4.57	4.70
A1	0.00	0.10	0.25
A2	2.59	2.69	2.79
b	0.77	-	0.90
b2	1.23	-	1.36
c	0.34	-	0.47
C2	1.22	-	1.32
D	9.05	9.15	9.25
D1	6.60	-	-
E	10.06	10.16	10.26
E1	7.80	-	8.20
e	2.54BSC		
H	14.70	15.10	15.50
L	2.00	2.30	2.60
L1	1.17	1.27	1.40
L2	-	-	1.75
L3	0.25 BSC		
L4	2.50REF		
Φ	0°		8°

TAPE AND REEL INFORMATION

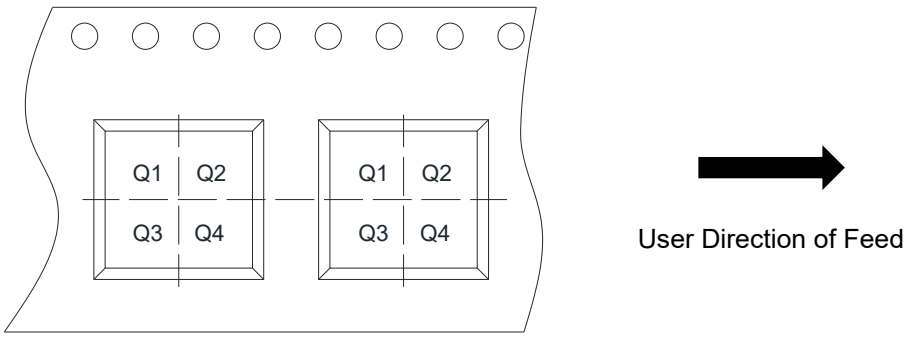
Reel Dimensions



Tape Dimensions



Quadrant Assignments For PIN1 Orientation In Tape



RD	Reel Dimension	☐ 7inch	☑ 13inch		
W	Overall width of the carrier tape	☐ 8mm	☐ 12mm	☐ 16mm	☑ 24mm
P1	Pitch between successive cavity centers	☐ 2mm	☐ 4mm	☐ 8mm	☑ 16mm
Pin1	Pin1 Quadrant	☐ Q1	☑ Q2	☐ Q3	☐ Q4