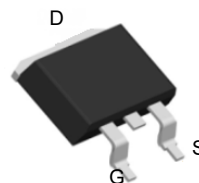


SNM102R3THA

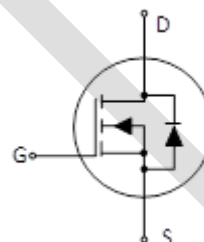
Single N-Channel, 100V, 120A, Power MOSFET

<http://www.sitcores.com/>

V_{DS} (V)	Max. $R_{DS(on)}$ (m Ω)
100	2.3@ $V_{GS}=10V$



TO-263-2L



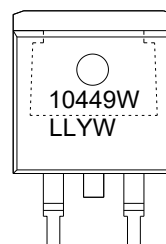
Description

The SNM102R3THA is N-Channel enhancement MOS Field Effect Transistor. Uses advanced Split Gate technology and design to provide excellent $R_{DS(on)}$ with low gate charge. This device is suitable for use in DC-DC conversion, power switch and charging circuit. Standard Product SNM102R3THA is in compliance with RoHS.

Features

- Split Gate Trench Technology
- Supper high density cell design
- Excellent ON resistance
- 100% UIS and Rg Tested
- High Robustness

Pin configuration (Top view)



10449W = Device Code
 LL = Special Code
 Y = Year
 W = Week (A~z)

Marking

Applications

- Hot swap
- Motor control and drive
- Battery management
- Load/Power Switching for portable device

Order information

Device	Package	Shipping
SNM102R3THA-2/TR	TO-263-2L	800/Tape&Reel

Absolute Maximum ratings

Parameter	Symbol	Maximum	Unit
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ^f	I_D	$T_C=25^{\circ}\text{C}$ 120	A
		$T_C=100^{\circ}\text{C}$ 120	A
Pulsed Drain Current ^c	I_{DM}	836	A
Continuous Drain Current ^a	I_{DSM}	$T_A=25^{\circ}\text{C}$ 69	A
		$T_A=70^{\circ}\text{C}$ 55	
Avalanche Energy $L=0.1\text{mH}$	E_{AS}	608	mJ
Power Dissipation ^b	P_D	$T_C=25^{\circ}\text{C}$ 375	W
		$T_C=100^{\circ}\text{C}$ 188	
Power Dissipation ^a	P_{DSM}	$T_A=25^{\circ}\text{C}$ 20.0	W
		$T_A=70^{\circ}\text{C}$ 12.7	
Operating Junction Temperature	T_J	-55 to 175	$^{\circ}\text{C}$
Storage Temperature Range	T_{STG}	-55 to 175	$^{\circ}\text{C}$

Thermal resistance ratings

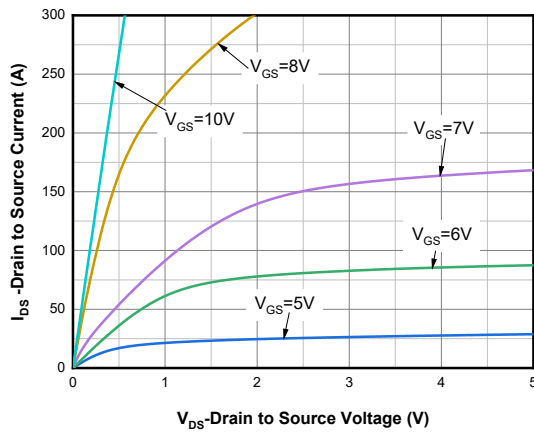
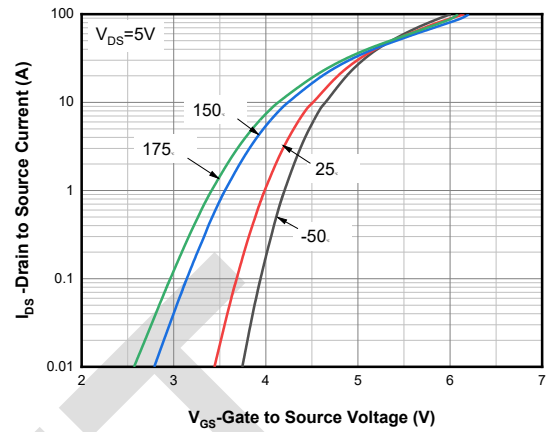
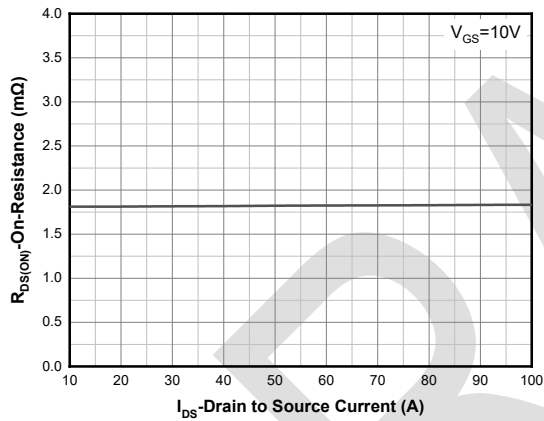
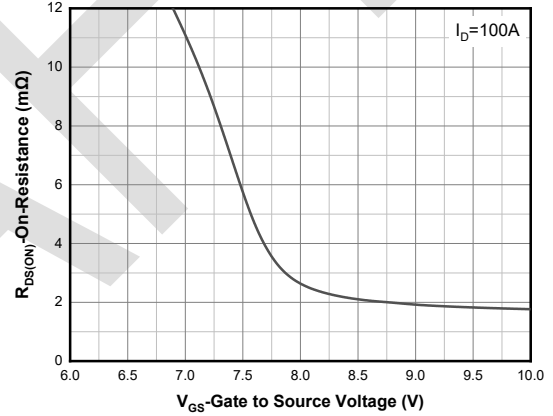
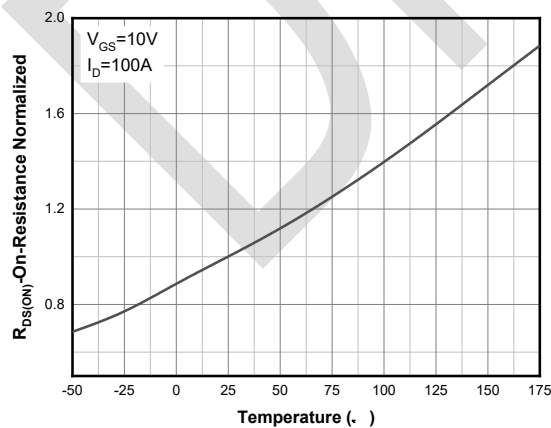
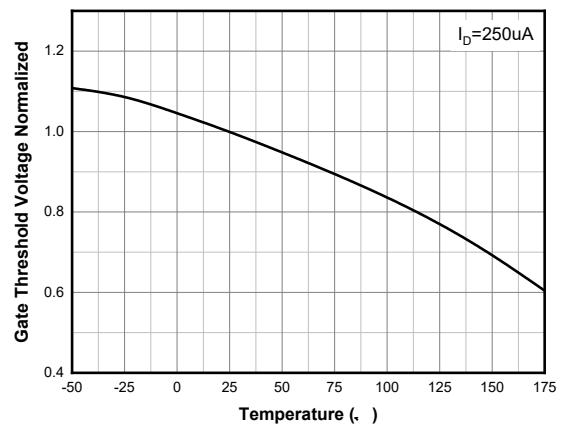
Single Operation					
Parameter		Symbol	Typical	Maximum	Unit
Junction-to-Ambient Thermal Resistance ^a	t ≤ 10 s	R _{θJA}	6	8	°C/W
	Steady State		33	43	
Junction-to-Case Thermal Resistance	Steady State	R _{θJC}	0.25	0.4	

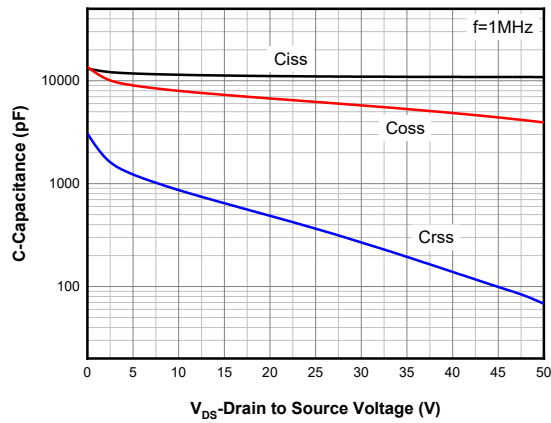
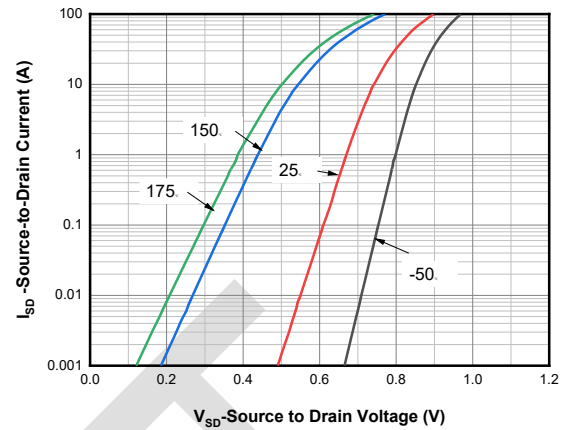
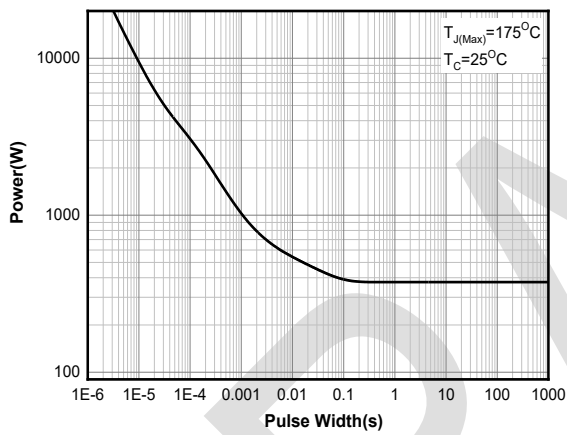
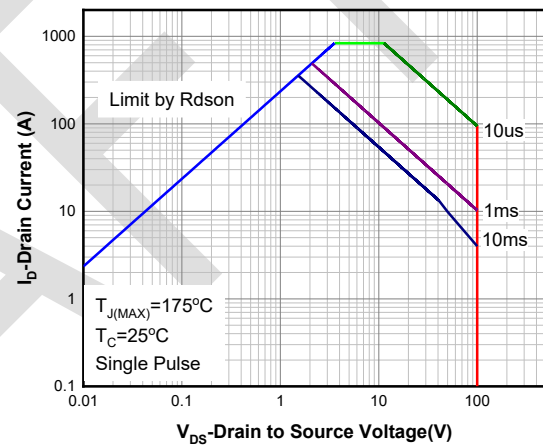
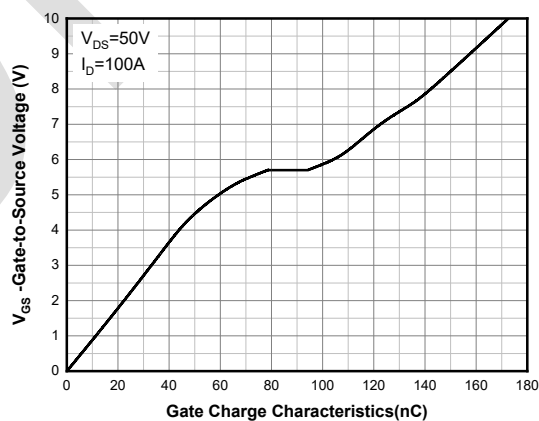
Note:

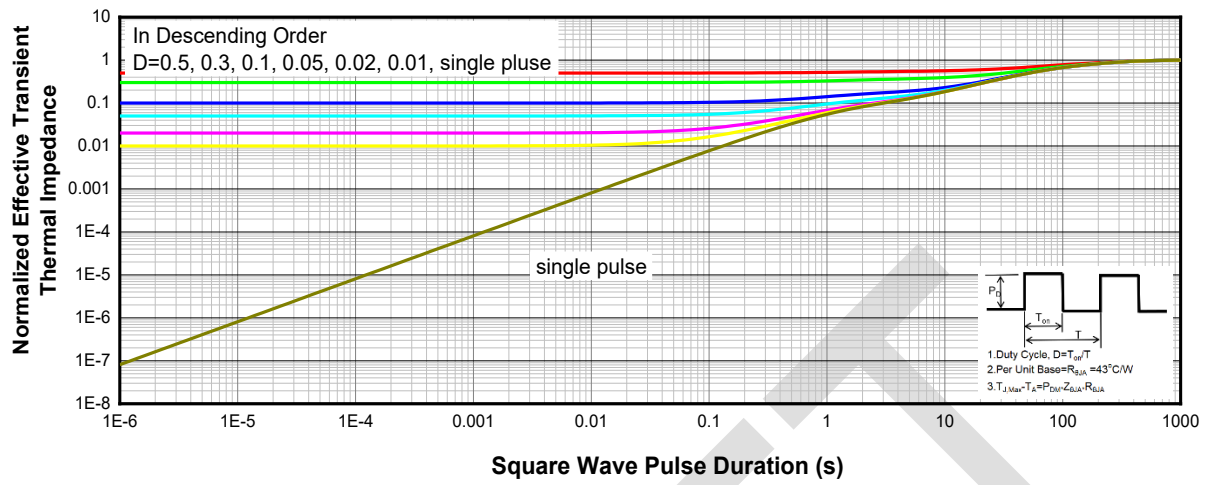
- a FR-4 board (38mm X 38mm X t1.6mm, 70um Copper) partially covered with copper (645mm² area). The power dissipation P_{DSM} is based on Junction-to-Ambient thermal resistance $R_{\theta JA}$ $t \leq 10\text{s}$ value and the $T_{J(MAX)}=175^{\circ}\text{C}$. The value is only for reference, any application depends on the user's specific board design.
- b The power dissipation P_D is based on $T_{J(MAX)}=175^{\circ}\text{C}$, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heat sinking is used.
- c Repetitive rating, ~10us pulse width, duty cycle ~1%, keep initial $T_J = 25^{\circ}\text{C}$, the maximum allowed junction temperature of 175°C .
- d The static characteristics are obtained using ~380us pulses, duty cycle ~1%.
- e The parameter is not subject to production test – verified by design / characterization.
- f The maximum current rating by source bonding technology.

Electronics Characteristics (Ta=25°C, unless otherwise noted)

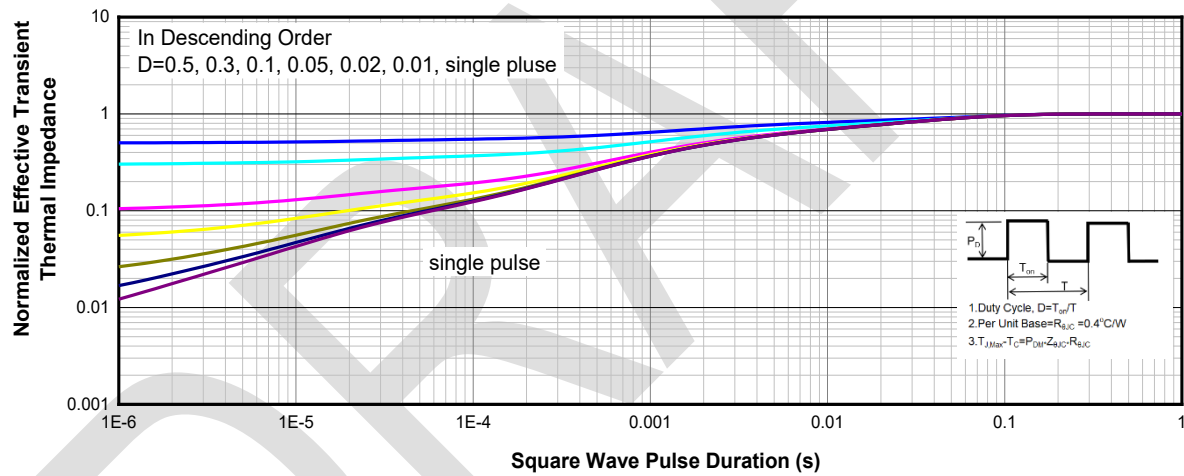
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0 V, I _D = 250uA	100			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 100V, V _{GS} = 0V			1	uA
Gate-to-source Leakage Current	I _{GSS}	V _{DS} = 0V, V _{GS} = ±20V			±100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = 250uA	2.5	3.0	3.5	V
Drain-to-source On-resistance ^d	R _{DS(on)}	V _{GS} = 10V, I _D =100A		1.8	2.3	mΩ
CHARGES, CAPACITANCES AND GATE RESISTANCE ^e						
Input Capacitance	C _{ISS}	V _{GS} = 0V, f = 1.0MHz, V _{DS} = 50 V		10858		pF
Output Capacitance	C _{OSS}			3936		
Reverse Transfer Capacitance	C _{RSS}			68		
Total Gate Charge(10V)	Q _{G(TOT)}	V _{GS} = 10 V,		171		nC
Gate-to-Source Charge	Q _{GS}	V _{DD} = 50V,		62		
Gate-to-Drain Charge	Q _{GD}	I _D = 100A		43		
Gate Resistance	R _g	f=1MHz		2.2		Ω
SWITCHING CHARACTERISTICS ^e						
Turn-On Delay Time	td(ON)	V _{GS} = 10 V, V _{DD} = 50 V, I _D =100A, R _G = 6Ω		56		ns
Rise Time	tr			190		
Turn-Off Delay Time	td(OFF)			114		
Fall Time	tf			130		
Body Diode Reverse Recovery Time	trr	I _F =20A, dI/dt=100A/μs		106		ns
Body Diode Reverse Recovery Charge	Qrr			300		nC
BODY DIODE CHARACTERISTIC						
Forward Voltage ^d	V _{SD}	V _{GS} = 0 V, I _S = 100A		0.9	1.2	V

Typical Characteristics (Ta=25°C, unless otherwise noted)

Output Characteristics ^d

Transfer Characteristics ^d

On-Resistance vs. Drain Current ^d

On-Resistance vs. Gate-to-Source Voltage ^d

On-Resistance vs. Junction Temperature ^d

Threshold Voltage vs. Temperature


Capacitance

Body Diode Forward Voltage^d

Single Pulse power

Safe Operating Area

Gate Charge Characteristics



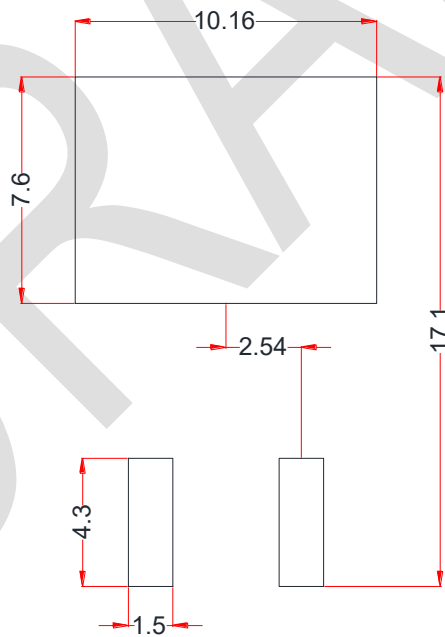
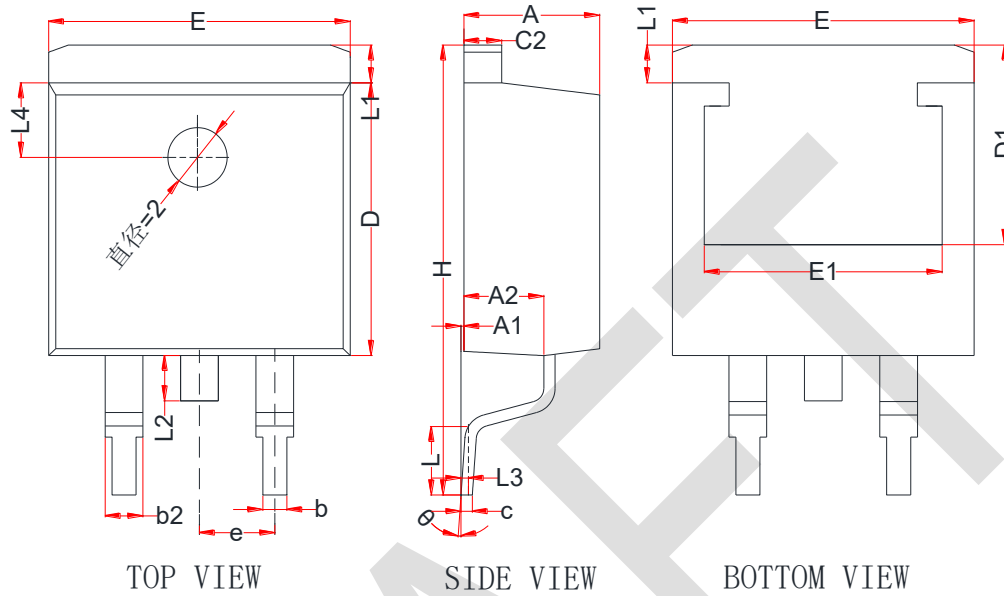
Transient Thermal Response (Junction-to-Ambient)



Transient Thermal Response (Junction-to-Case)

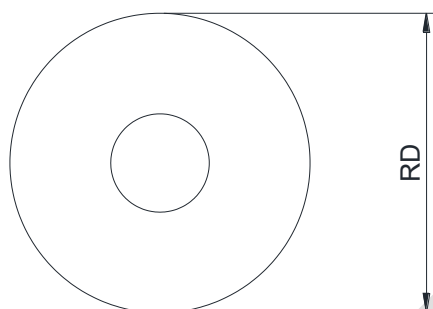
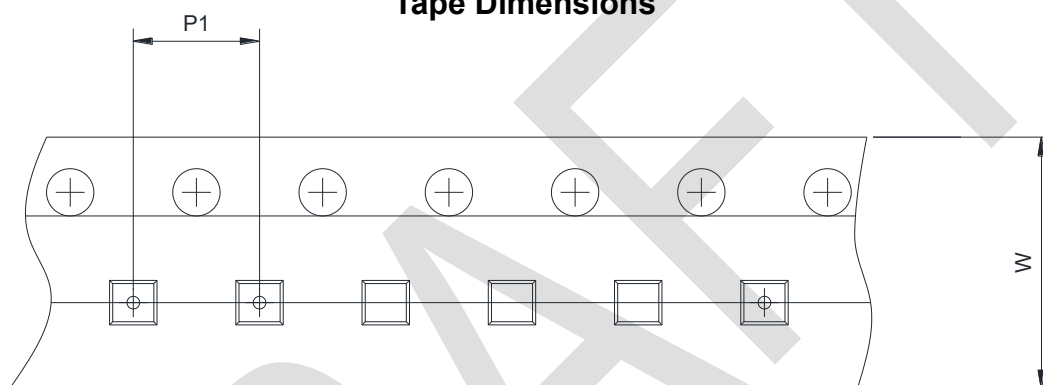
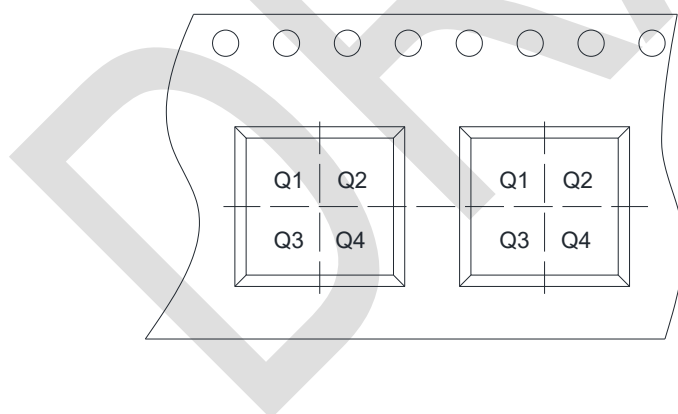
PACKAGE OUTLINE DIMENSIONS

TO-263-2L



RECOMMENDED LAND PATTERN (Unit:mm)

Symbol	Dimensions in Millimeters		
	Min.	Typ.	Max.
A	4.40	4.57	4.70
A1	0.00	0.10	0.25
A2	2.59	2.69	2.79
b	0.77	-	0.90
b2	1.23	-	1.36
c	0.34	-	0.47
C2	1.22	-	1.32
D	9.05	9.15	9.25
D1	6.60	-	-
E	10.06	10.16	10.26
E1	7.80	-	8.20
e	2.54BSC		
H	14.70	15.10	15.50
L	2.00	2.30	2.60
L1	1.17	1.27	1.40
L2	-	-	1.75
L3	0.25 BSC		
L4	2.50REF		
Φ	0°		8°

TAPE AND REEL INFORMATION
Reel Dimensions

Tape Dimensions

Quadrant Assignments For PIN1 Orientation In Tape


User Direction of Feed

RD	Reel Dimension	☐ 7inch	☒ 13inch		
W	Overall width of the carrier tape	☐ 8mm	☐ 12mm	☐ 16mm	☒ 24mm
P1	Pitch between successive cavity centers	☐ 2mm	☐ 4mm	☐ 8mm	☒ 16mm
Pin1	Pin1 Quadrant	☐ Q1	☒ Q2	☐ Q3	☐ Q4