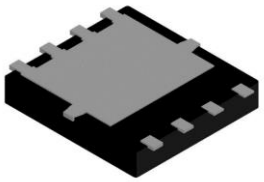
SNM103R4DNA

Single N-Channel, 100V,155A Power MOSFET

http://www.sitcores.com/

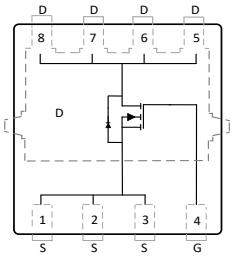
V_{DS} (V)	Max. $R_{DS(on)}$ (mΩ)
100	3.4 @ V_{GS}=10V



PDFN5X6-8L

Descriptions

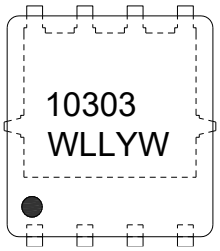
The SNM103R4DNA is N-Channel enhancement MOS Field Effect Transistor. Uses advanced split gate Trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. This device is suitable for use in DC-DC conversion, power switch and charging circuit. Standard Product SNM103R4DNA is Pb-free.



Pin configuration (Top view)

Features

- Split Gate Trench Technology
- Supper high density cell design
- Excellent ON resistance
- High Robustness
- 100% Rg and Avalanche Tested
- MSL1



10303 = Device Code
WLL = Special Code
Y = Year
W = Week (A~z)

Marking

Applications

- Hot swap
- Motor control and drive
- Battery management
- Load/Power Switching for portable device

Order information

Device	Package	Shipping
SNM103R4DNA-8/TR	PDFN5X6-8L	5000/Tape&Reel

Absolute Maximum ratings

Parameter		Symbol	Maximum	Unit
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current	T_C=25°C	I_D	155	A
	T_C=100°C		110	A
Pulsed Drain Current [c]		I_{DM}	325	A
Continuous Drain Current	T_A=25°C	I_{DSM}	28	A
	T_A=70°C		32	
Avalanche Energy L=0.3mH		E_{AS}	408	mJ
Power Dissipation [b]	T_C=25°C	P_D	167	W
	T_C=100°C		83	
Power Dissipation [a]	T_A=25°C	P_{DSM}	10	W
	T_A=70°C		7	
Operating Junction Temperature		T_J	-55 to 175	°C
Storage Temperature Range		T_{STG}	-55 to 175	°C

Thermal resistance ratings

Single Operation					
Parameter		Symbol	Typical	Maximum	Unit
Junction-to-Ambient Thermal Resistance [a]	t ≤ 10 s	$R_{\theta JA}$	12	15	°C/W
	Steady State		39	47	
Junction-to-Case Thermal Resistance	Steady State	$R_{\theta JC}$	0.6	0.9	

Note:

a FR-4 board (38mm X 38mm X t1.6mm, 70um Copper) partially covered with copper (645mm^2 area). The power dissipation P_{DSM} is based on Junction-to-Ambient thermal resistance $R_{\theta JA}$ t≤10s value and the $T_{J(MAX)}$=175°C. The value is only for reference, any application depends on the user's specific board design.

b The power dissipation P_D is based on $T_{J(MAX)}$=175°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heat sinking is used.

c Repetitive rating, ~10us pulse width, duty cycle ~1%, keep initial T_J =25°C, the maximum allowed junction temperature of 175°C.

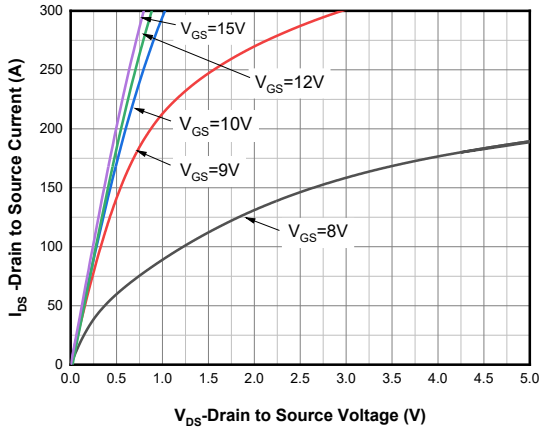
d The static characteristics are obtained using ~380us pulses, duty cycle ~1%.

e The parameter is not subject to production test – verified by design / characterization.

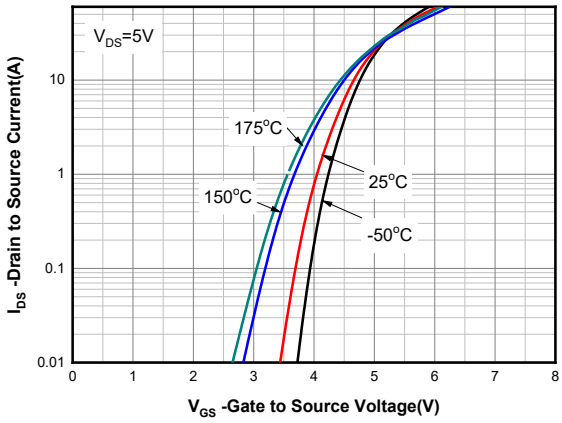
Electronics Characteristics (Ta=25°C, unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0 V, I_D = 250uA	100			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 100 V, V_{GS} = 0V			1	uA
Gate-to-source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20V			±100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250uA	2.5	3.0	3.5	V
Drain-to-source On-resistance [d]	$R_{DS(on)}$	V_{GS} = 10V, I_D = 20A		2.7	3.4	mΩ
CHARGES, CAPACITANCES AND GATE RESISTANCE [e]						
Input Capacitance	C_{ISS}	V_{GS} = 0 V, f = 1.0MHz, V_{DS} = 50 V		4560		pF
Output Capacitance	C_{OSS}			1800		
Reverse Transfer Capacitance	C_{RSS}			31		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} =10V, V_{DD} = 50V, I_D = 20A		72		nC
Gate-to-Source Charge	Q_{GS}			22		
Gate-to-Drain Charge	Q_{GD}			16		
Gate Resistance	R_g	f=1MHz		1.7		Ω
SWITCHING CHARACTERISTICS [e]						
Turn-On Delay Time	td(ON)	V_{GS} = 10V, V_{DD} = 50V, I_D =20 A , R_G=3Ω		16		ns
Rise Time	tr			27		
Turn-Off Delay Time	td(OFF)			40		
Fall Time	tf			22		
BODY DIODE CHARACTERISTICS						
Body Diode Reverse Recovery Time	trr	I_F=20A, dI/dt=100A/μs		83		ns
Body Diode Reverse Recovery Charge	Qrr			130		nC
Forward Voltage [d]	V_{SD}	V_{GS} = 0 V, I_S = 20A		0.8	1.2	V

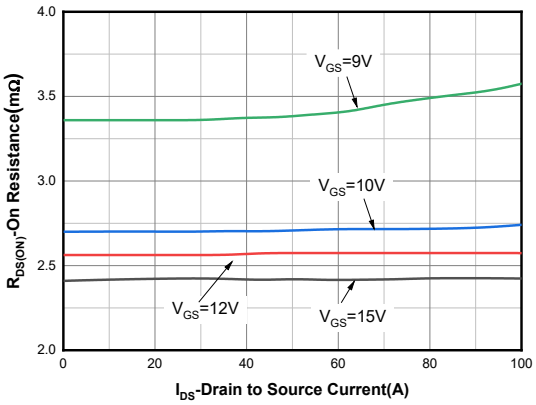
Typical Characteristics (Ta=25°C, unless otherwise noted)



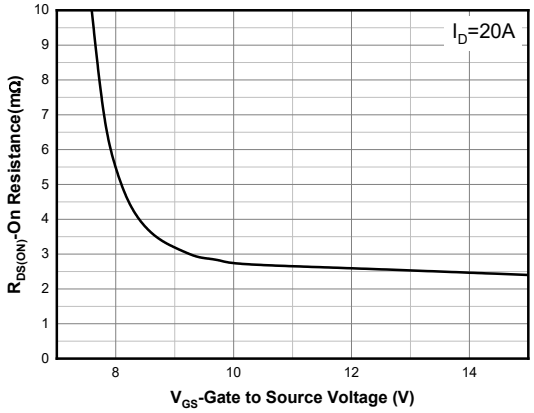
Output Characteristics [d]



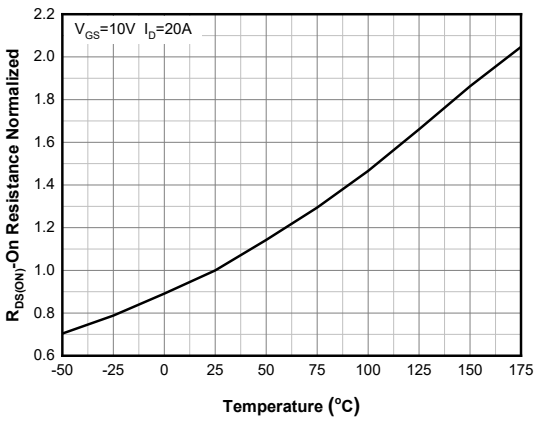
Transfer Characteristics [d]



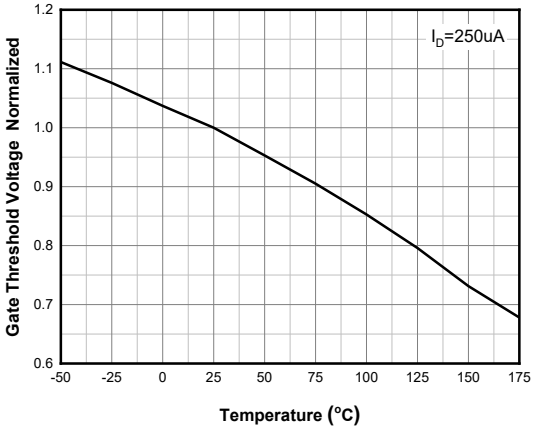
On-Resistance vs. Drain Current [d]



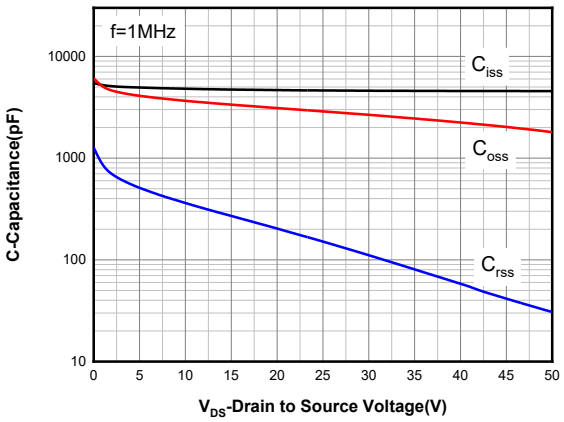
On-Resistance vs. Gate to Source Voltage [d]



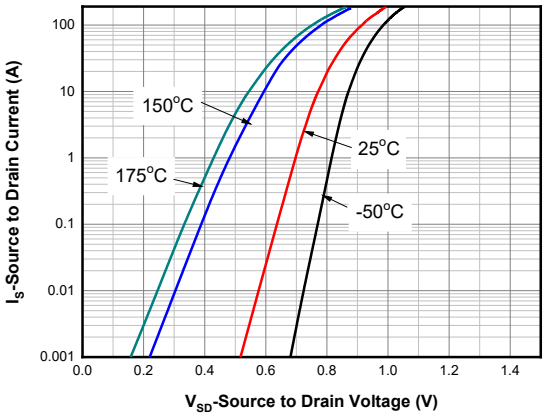
On-Resistance vs. Junction Temperature [d]



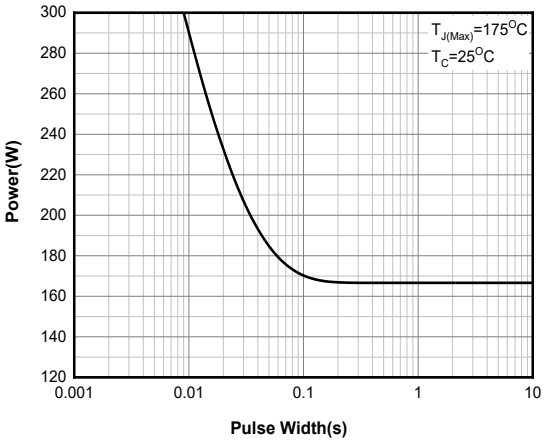
Threshold Voltage vs. Temperature



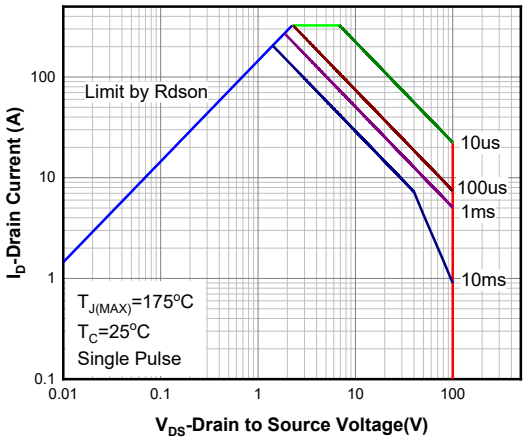
Capacitance



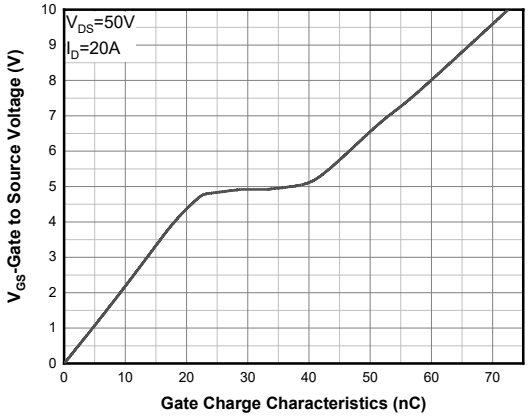
Body Diode Forward Voltage [d]



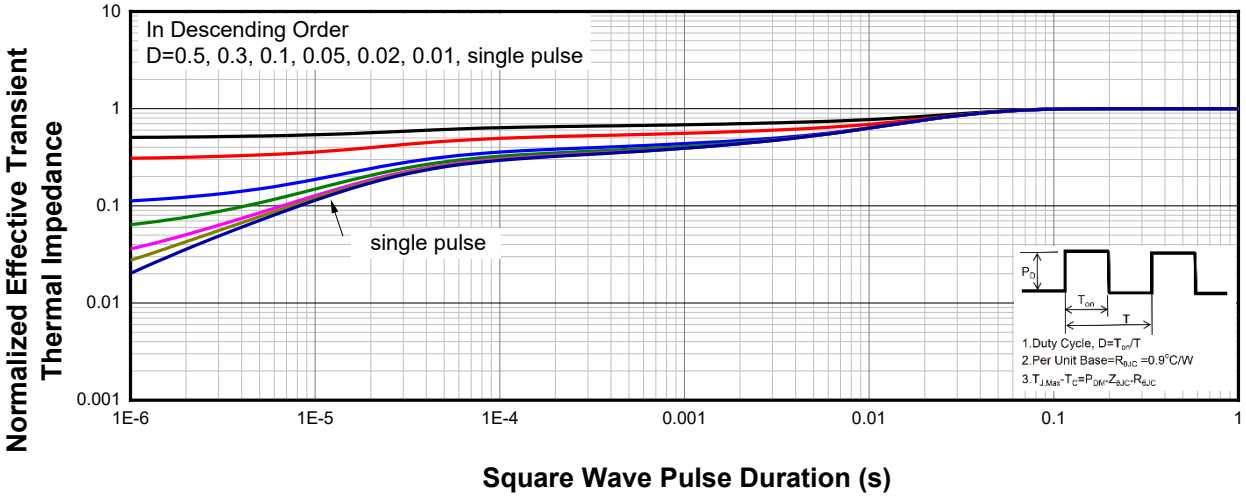
Single Pulse Power



Safe Operating Area

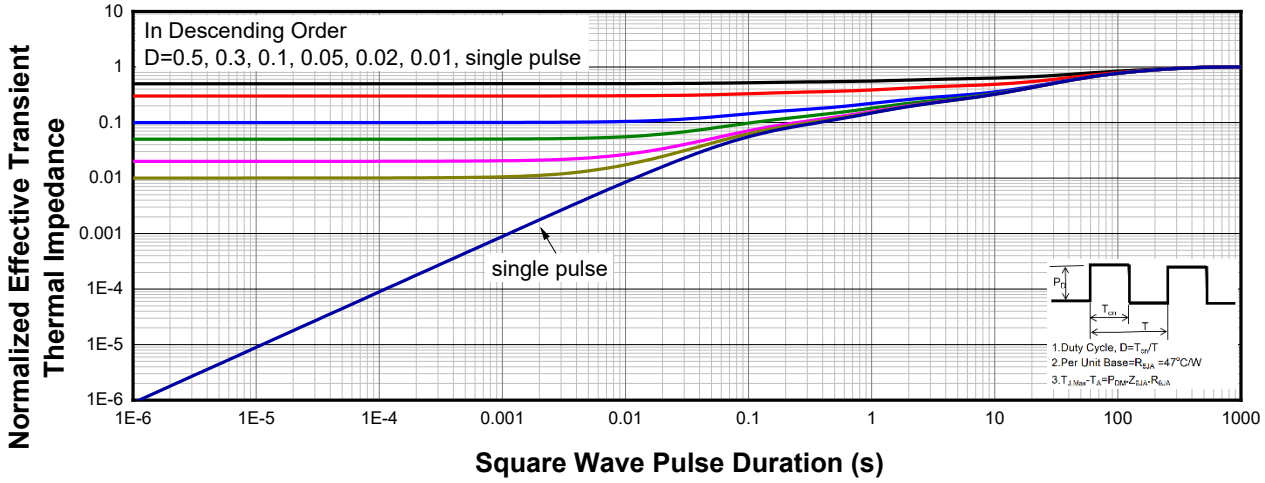


Gate Charge Characteristics



Square Wave Pulse Duration (s)

Transient Thermal Response (Junction-to-Case)

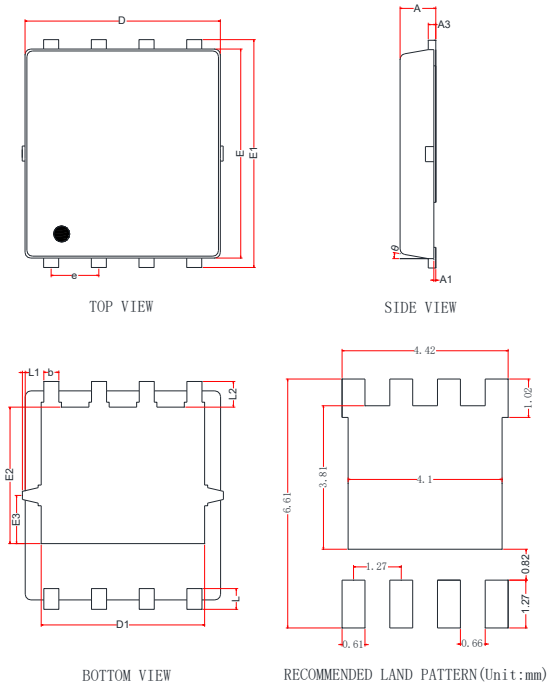


Square Wave Pulse Duration (s)

Transient Thermal Response (Junction-to-Ambient)

PACKAGE OUTLINE DIMENSIONS

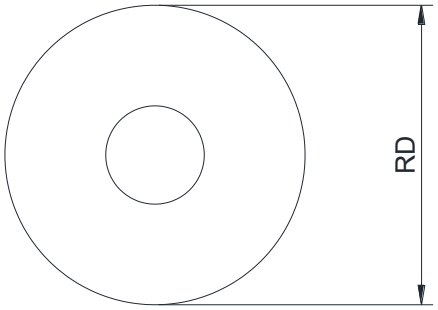
PDFN5x6-8L



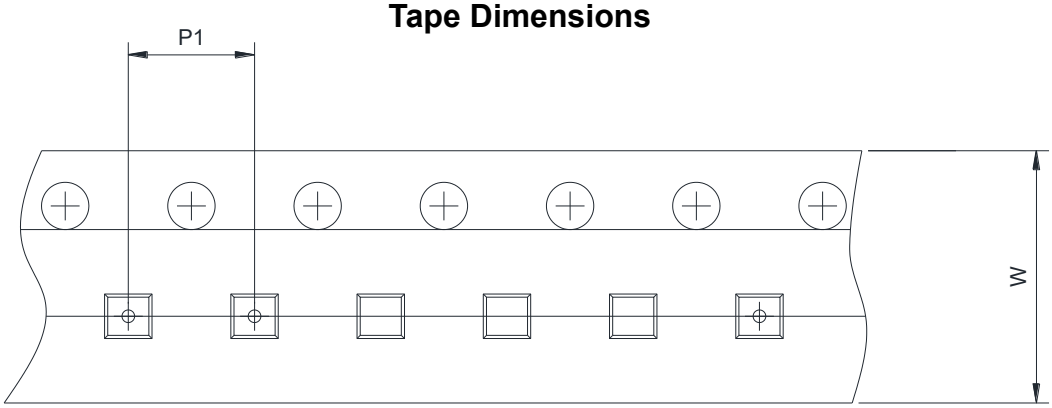
Symbol	Dimensions in Millimeters		
	Min.	Typ.	Max.
A	0.85	0.95	1.00
A1	0.00	---	0.05
A3	---	0.2 Ref	---
b	0.30	0.40	0.50
D	5.10	5.20	5.30
E	5.45	5.55	5.65
e	1.27 BSC		
D1	4.25	4.35	4.45
E1	5.95	6.05	6.15
E2	3.525	3.625	3.725
E3	1.175	1.275	1.375
L	0.45	0.55	0.65
L1	0	---	0.15
L2	0.68 Ref		
θ	0 °	---	10 °

TAPE AND REEL INFORMATION

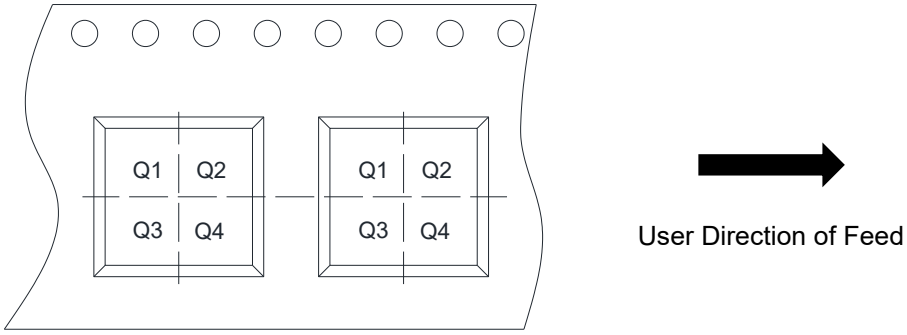
Reel Dimensions



Tape Dimensions



Quadrant Assignments For PIN1 Orientation In Tape



RD	Reel Dimension	☐ 7inch	☑ 13inch		
W	Overall width of the carrier tape	☐ 8mm	☑ 12mm	☐ 16mm	
P1	Pitch between successive cavity centers	☐ 2mm	☐ 4mm	☑ 8mm	
Pin1	Pin1 Quadrant	☑ Q1	☐ Q2	☐ Q3	☐ Q4