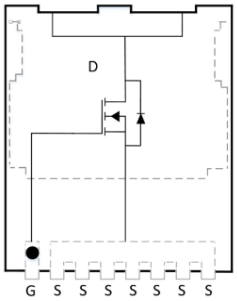
SNM156R6TLA

Single N-Channel, 150V,158A, Power MOSFET

http://www.sitcores.com/

V_{DS} (V)	Max. $R_{DS(on)}$ (mΩ)
150	6.6@ V_{GS}=10V

TOLL-8L



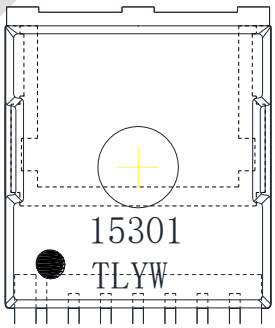
Pin configuration (Top view)

Description

The SNM156R6TLA is N-Channel enhancement MOS Field Effect Transistor. Uses advanced Split Gate Trench and design to provide excellent $R_{DS(ON)}$ with low gate charge. This device is suitable for use in DC-DC conversion, power switch and charging circuit. Standard Product SNM156R6TLA is Pb-free.

Features

- Split Gate Trench Technology
- Supper high density cell design
- Excellent ON resistance
- Extremely Low Threshold Voltage
- Package TOLL-8L
- 100% UIS and Rg Tested
- MSL1



15301 = Device Code
TL = Special Code
Y = Year
W = Week(A~z)

Marking

Applications

- DC/DC converters
- Power supply converters circuit
- Load/Power Switching for portable device

Order information

Device	Package	Shipping
SNM156R6TLA-8/TR	TOLL-8L	1800/Tape&Reel

Absolute Maximum ratings

Parameter		Symbol	Maximum	Unit
Drain-Source Voltage		V_{DS}	150	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current	T_C=25°C	I_D	158	A
	T_C=100°C		112	A
Pulsed Drain Current [c]		I_{DM}	421	A
Continuous Drain Current	T_A=25°C	I_{DSM}	31	A
	T_A=70°C		26	
Avalanche Energy L=0.3mH		E_{AS}	760	mJ
Power Dissipation [b]	T_C=25°C	P_D	429	W
	T_C=100°C		214	
Power Dissipation [a]	T_A=25°C	P_{DSM}	16.7	W
	T_A=70°C		11.7	
Operating Junction Temperature		T_J	-55 to 175	°C
Storage Temperature Range		T_{STG}	-55 to 175	°C

Thermal resistance ratings

Single Operation					
Parameter		Symbol	Typical	Maximum	Unit
Junction-to-Ambient Thermal Resistance [a]	t ≤ 10 s	$R_{\theta JA}$	7	9	°C/W
	Steady State		29	38	
Junction-to-Case Thermal Resistance	Steady State	$R_{\theta JC}$	0.24	0.35	

Note:

a FR-4 board (38mm X 38mm X t1.6mm, 70um Copper) partially covered with copper (645mm^2 area). The power adissipation P_{DSM} is based on Junction-to-Ambient thermal resistance $R_{\theta JA}$ t≤10s value and the $T_{J(MAX)}$=175°C. The value is only for reference, any application depends on the user's specific board design.

b The power dissipation P_D is based on $T_{J(MAX)}$=175°C, using junction-to-case thermal resistance, and is more useful in asetting the upper dissipation limit for cases where additional heat sinking is used.

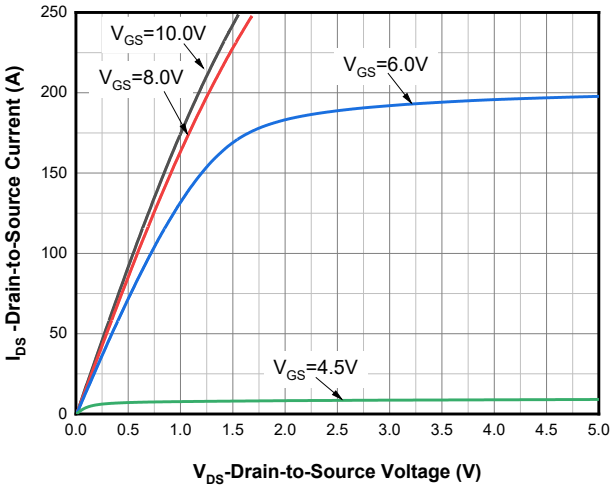
c Repetitive rating, ~10us pulse width, duty cycle ~1%, keep initial T_J =25°C, the maximum allowed junction temperature of 175°C.

d The static characteristics are obtained using ~380us pulses, duty cycle ~1%.

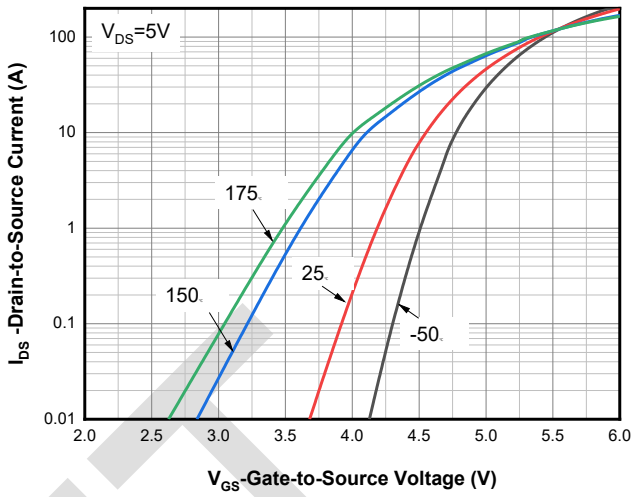
e The parameter is not subject to production test – verified by design / characterization.

Electronics Characteristics (Ta=25°C, unless otherwise noted)

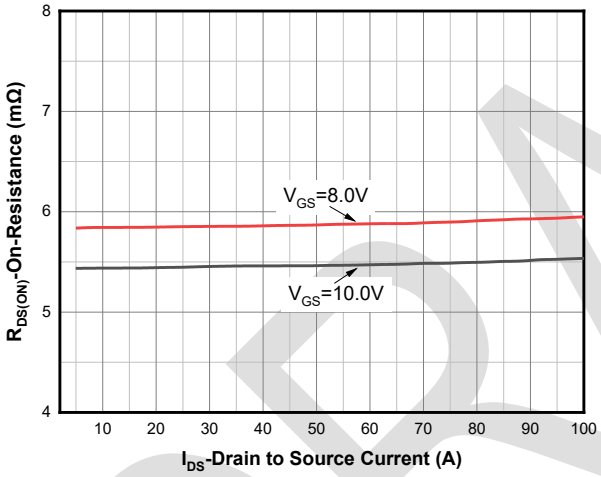
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0 V, I_D = 250uA	150			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} =150V, V_{GS} = 0V			1	uA
Gate-to-source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20V			±100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250uA	2.6	3.2	3.8	V
Drain-to-source On-resistance [d]	$R_{DS(on)}$	V_{GS} =10V, I_D =20A		5.3	6.6	mΩ
CHARGES, CAPACITANCES AND GATE RESISTANCE [e]						
Input Capacitance	C_{ISS}	V_{GS} = 0V, f = 1.0MHz, V_{DS} = 75 V		4986		pF
Output Capacitance	C_{OSS}			579		
Reverse Transfer Capacitance	C_{RSS}			19		
Total Gate Charge	$Q_{G(10V)}$	V_{GS} =10V, V_{DD} = 75V, I_D =20A		68		nC
Total Gate Charge	$Q_{G(8V)}$			54		
Gate-to-Source Charge	Q_{GS}			23		
Gate-to-Drain Charge	Q_{GD}			12		
Gate Resistance	R_g	f=1MHz		2.1		Ω
SWITCHING CHARACTERISTICS [e]						
Turn-On Delay Time	td(ON)	V_{GS} =10V, V_{DD}= 75V, I_D=20A, R_G=3Ω		16.5		ns
Rise Time	tr			19.9		
Turn-Off Delay Time	td(OFF)			47.0		
Fall Time	tf			18.7		
BODY DIODE CHARACTERISTICS						
Body Diode Reverse Recovery Time	trr	I_F=20A,dI/dt=100A/μs		102		ns
Body Diode Reverse Recovery Charge	Qrr	I_F=20A,dI/dt=100A/μs		505		nC
Forward Voltage [d]	V_{SD}	V_{GS} = 0 V, I_S = 1A		0.7	1.2	V



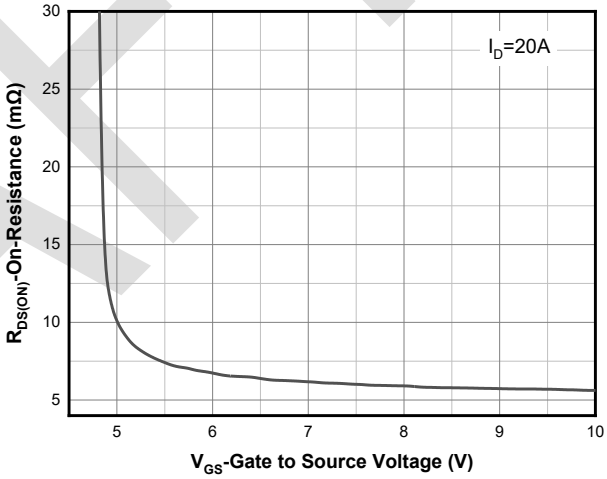
Output Characteristics [d]



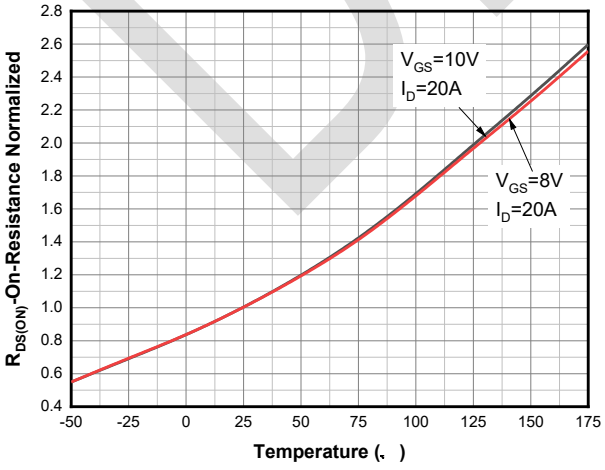
Transfer Characteristics [d]



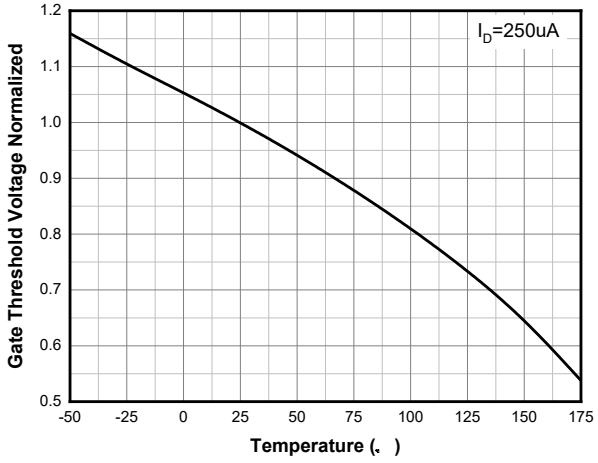
On-Resistance vs. Drain Current [d]



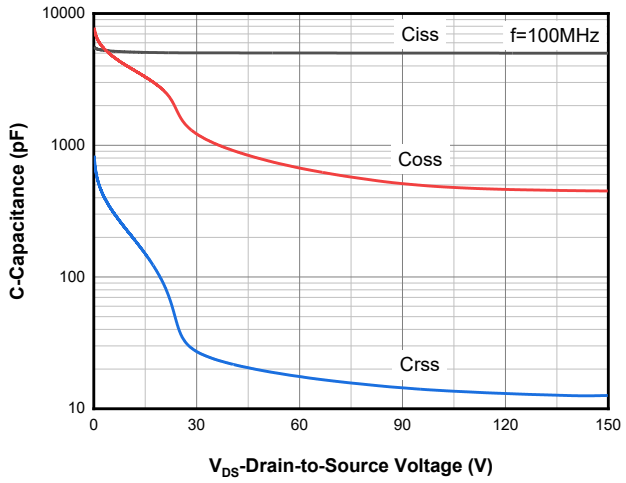
On-Resistance vs. Gate-to-Source Voltage [d]



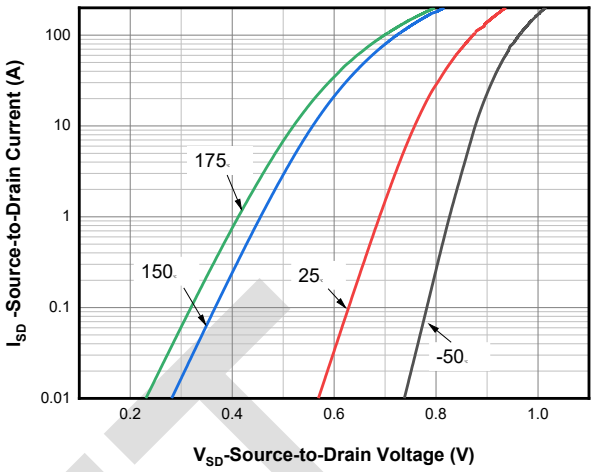
On-Resistance vs. Junction Temperature [d]



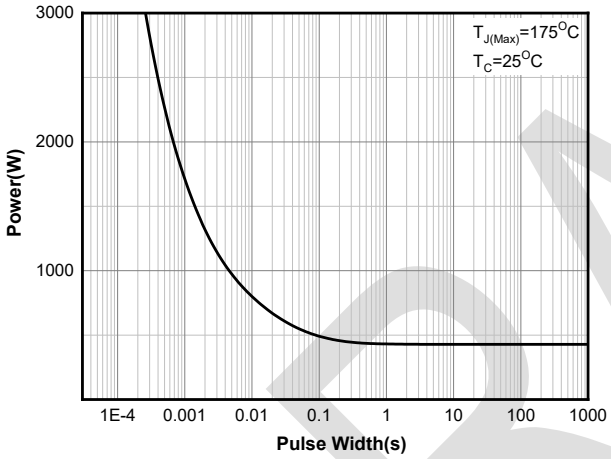
Threshold Voltage vs. Temperature



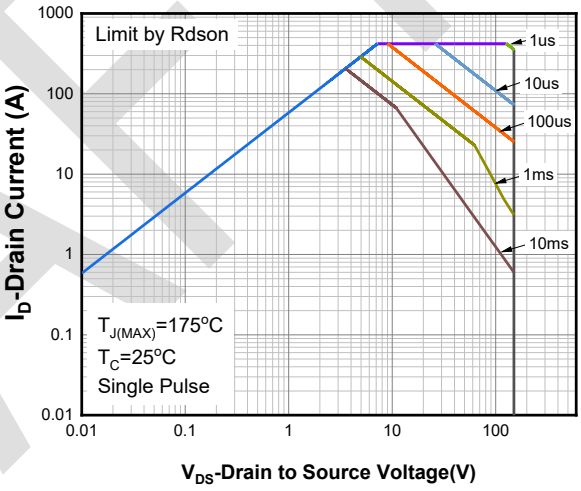
Capacitance



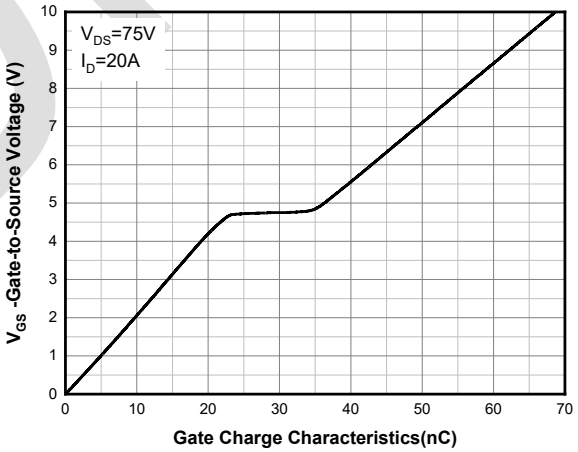
Body Diode Forward Voltage [d]



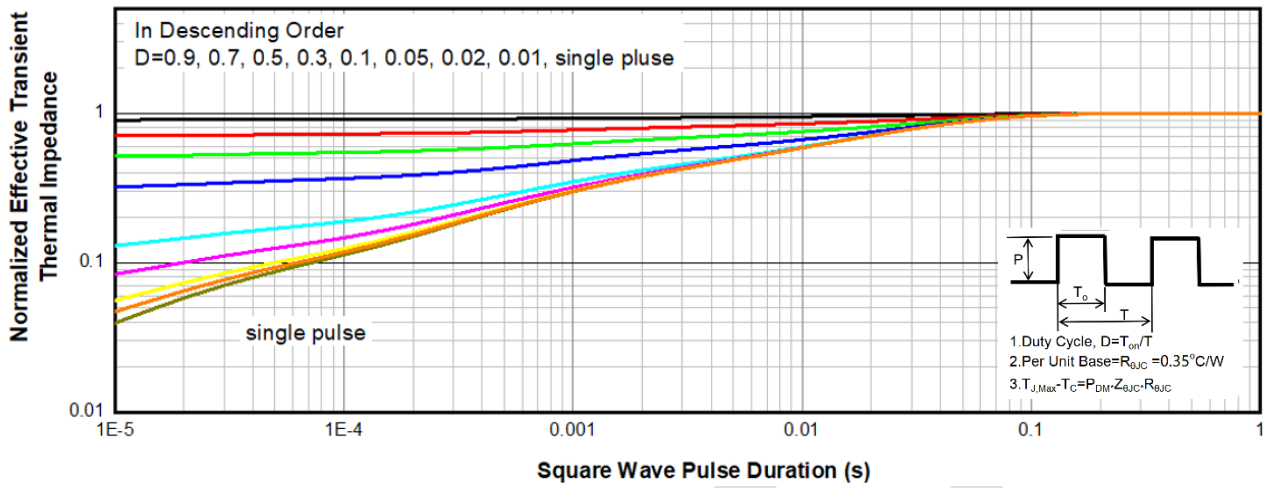
Single Pulse power



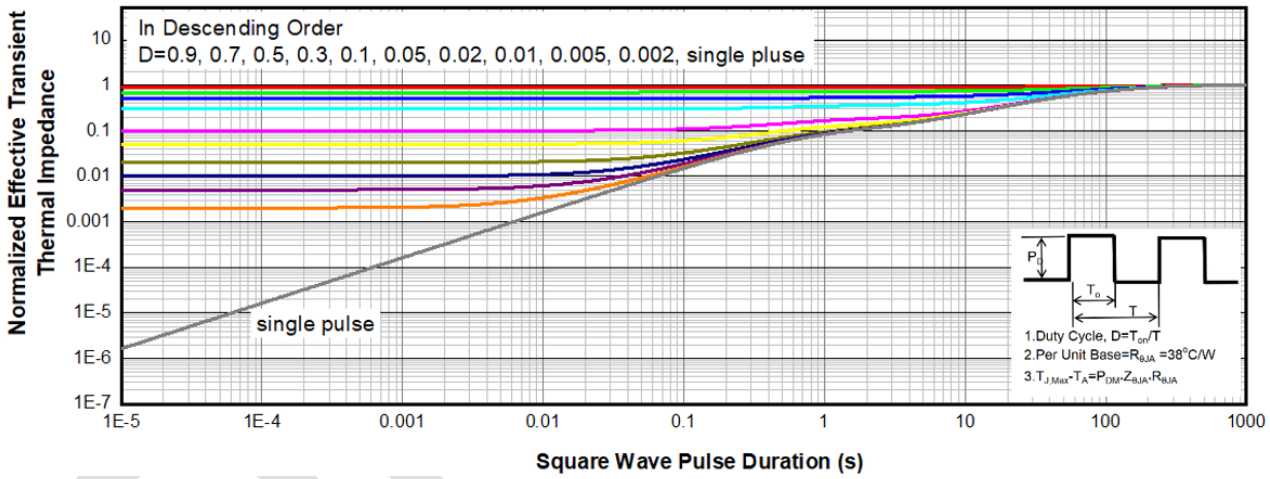
Safe Operating Area



Gate Charge Characteristics



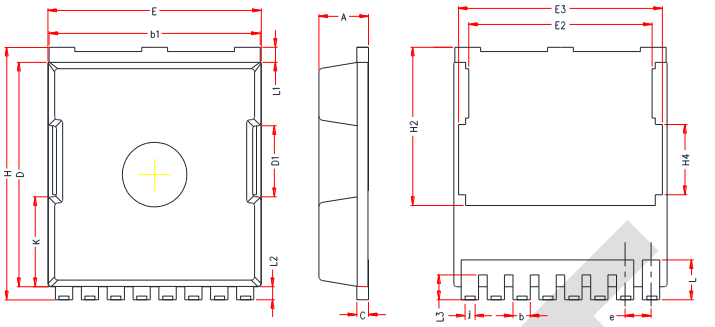
Transient Thermal Response (Junction-to-Case)



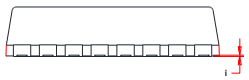
Transient Thermal Response (Junction-to-Ambient)

PACKAGE OUTLINE DIMENSIONS

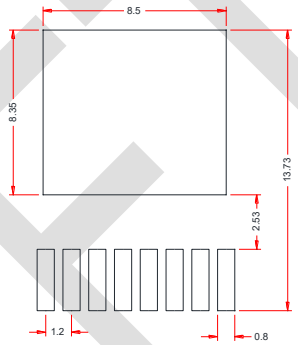
TOLL-8L



TOP VIEW SIDE VIEW BOTTOM VIEW



SIDE VIEW

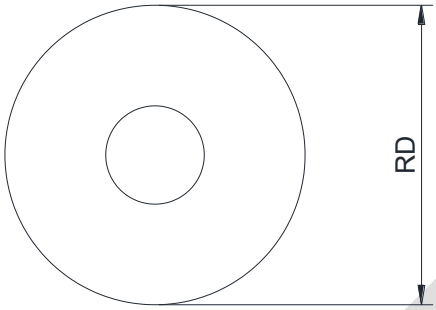


RECOMMOND LAND PATTERN(Unit：mm）

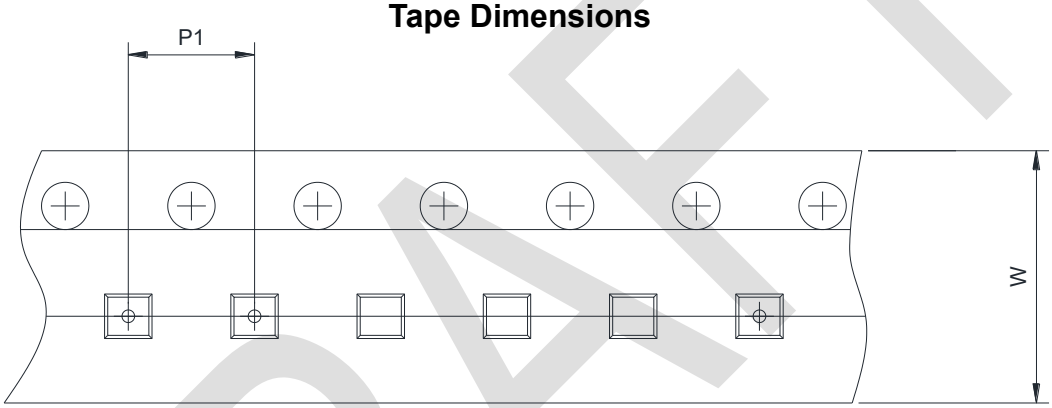
Symbol	Dimensions in Millimeters		
	Min.	Typ.	Max.
A	2.20	2.30	2.40
b	0.70	0.80	0.90
b1	9.70	9.80	9.90
c	0.40	0.50	0.60
D	10.28	10.38	10.48
D1	3.20	3.30	3.40
E	9.80	9.90	10.00
E2	8.40	8.50	8.60
E3	9.30	9.40	9.50
e	1.20 BASIC		
H	11.58	11.68	11.78
H2	7.23	7.33	7.43
H4	3.16	3.26	3.36
K	4.08	4.18	4.28
L	1.60	1.90	2.10
L1	0.60	0.70	0.80
L2	0.50	0.60	0.70
L3	1.05	1.20	1.30
i	0.10	-	-
j	0.45 Ref		

TAPE AND REEL INFORMATION

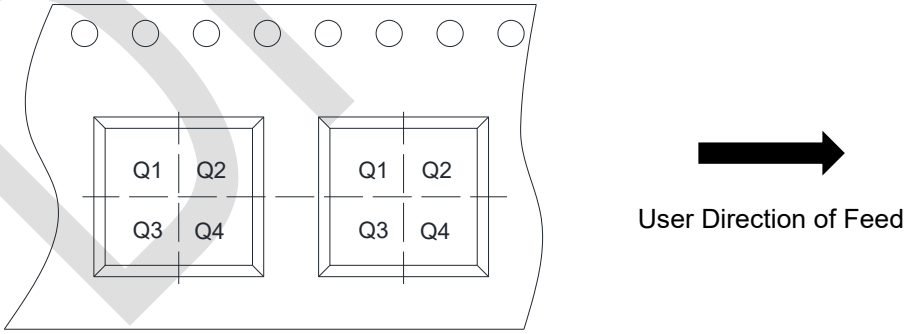
Reel Dimensions



Tape Dimensions



Quadrant Assignments For PIN1 Orientation In Tape



RD	Reel Dimension	☐ 7inch	☑ 13inch		
W	Overall width of the carrier tape	☐ 8mm	☐ 12mm	☐ 16mm	☑ 24mm
P1	Pitch between successive cavity centers	☐ 2mm	☐ 4mm	☐ 8mm	☑ 12mm
Pin1	Pin1 Quadrant	☐ Q1	☑ Q2	☐ Q3	☐ Q4